BCS PROFESSIONAL EXAMINATIONS
BCS Level 5 Diploma in IT

April 2008

EXAMINERS' REPORT

Computer Architecture

General Comments

Students as in previous years were very selective in answering questions. The favourites questions were on logic circuits, computer architecture, and memory with some focus on instructions and addressing modes. This is the last year of offer of this unit and these days of Internet and multimedia software and systems, computer hardware is hardly a favourite subject.

Question 1

For the function:

f = A'B'C'D'+ A'BCD' + ABD + AC'D + A'B'D' + AB'C' + AB'CD

a) Construct a Karnaugh map and use it to find a minimum sum of products expression for f.

(4 marks)

b) Draw a logic circuit for the minimised expression using only AND, OR and NOT gates.

(4 marks)

c) Manipulate the minimised expression for f into a form which does not use the AND operator and hence draw a logic circuit for f using only NOR gates.

(5 marks)

d) Manipulate the minimised expression for f into a form which does not use the OR operator and hence draw a logic circuit for f using only NAND gates.

(5 marks)

e) Compare the relative merits of the logic circuit solutions to parts b, c and d.

(3 marks)

f) Discuss the relative merits of implementing the circuit for f as a VLSI chip.

(4 marks)

Answer Pointers

a) f = AD + A'CD' + A'B'D' (or B'C'D')

b) 3 AND, 1 OR and 3 NOT gates. 3 gate propagation delays.

c) f = (A'+ D')' + (A + C' + D)' + (A + B + D)'

8 NOR gates. 4 gate propagation delays.

d) f = ((AD)' . (A'CD')' . (A'B'D')')'

7 NAND gates. 3 gate propagation delays.

e) Comparison should be based on the number of gates and propagation delays.

f) Too simple to implement on its own in VLSI. Considerable overheads in production time and cost.

Examiner's Guidance Notes

A number of candidates attempted this question and a few ran into problems in parts e) and f). The former were able to offer a provide comparison and briefly discuss issues in VLSI as well as time and cost overheads.

Question 2

a) The count sequence for a synchronous modulo six counter is shown in the table below:

state	Q2	Q1	Q0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1

i) By means of Karnaugh maps derive the minimised sum of products expressions for each stage of the counter if it is to be built from D type flipflops.

(7 marks)

ii) By means of Karnaugh maps derive the minimised sum of products expressions for each stage of the counter if it is to be built from JK type flipflops.

(7 marks)

iii) Draw the logic circuit for each of your counter designs and compare their relative merits.

(11 marks)

Answer Pointers

i) MSB $D_2 = Q_2 . Q_0' + Q_1 . Q_0$
MSB-1 $D_1 = Q_1 . Q_0' + Q_2' . Q_1' . Q_0$
LSB $D_0 = Q_0'$

ii) MSB $J_2 = Q_1 . Q_0$ $K_2 = Q_0$
MSB-1 $J_1 = Q_2'. Q_0$ $K_1 = Q_0$
LSB $J_0 = 1$ $K_0 = 1$

iii) The comparison should be based on speed and the number of extra logic gates above those required for the flip flops themselves.

Examiner's Guidance Notes

The responses here were mixed. While all those who attempted this question were able to answer i) and ii), most had difficulties in producing the comparison and in particular the issues on which the comparison should be based.

Question 3

a) Briefly discuss the memory hierarchy of a conventional digital computer in terms of access time and capacity.

(7 marks)

b) The strategy known as cache is used to enhance the performance of computer memory. Discuss its principles of operation and explain why it is so successful at reducing main store memory access times.

(12 marks)

c) Compare the cache memory strategy with that of virtual memory.

(6 marks)

Answer Pointers

a) A comparison should be drawn between the size and speed of the different elements of memory. At one end of the scale are the very low capacity but high speed processor registers. The hierarchy moves to slower speed and higher capacity via caches, main store through to disk and tape backing store.

b) Cache memory is of higher speed but lower capacity than main store. When an item of data or an instruction is required by the processor the cache is searched to see if it can be retrieved immediately from there. If so it can be passed to the processor with the faster access time offered by the cache. If not a cache miss is said to have occurred and the required item is fetched from main store and copied into the cache. The items held in cache have a tag to identify them. These tags are searched in parallel to ensure a high speed response to a data request. There are several ways of mapping items into cache and one of these strategies should be discussed. When the processor writes back to memory time is saved if the data is held in cache but a strategy for ensuring main memory is updated must be described. When the cache becomes full there must be a strategy on replacement such as least recently used. Cache is such a successful technique because of the temporal and spatial locality of memory accesses. Object code is usually stored sequentially in memory and because of loop constructs it is often reused many times over a short period. Data structures often use coherent blocks of memory and the variables they contain are frequently updated.

c) The two strategies share common principles in that both seek to interpose a small higher speed memory between the processor and a larger, slower memory. Both derive

benefit from the spatial and temporal locality of data and instructions. Both require a strategy to handle a miss when the required item is not available in the higher speed memory and to determine what should be replaced in higher speed memory when it becomes full. The major difference is that cache is faster than main store whereas virtual memory bridges the speed gap between main store and disk. When an item is not found in main store during a virtual memory access a page fault is said to have occurred and the time penalty is very much greater than when a miss occurs in cache. A very different approach is used to handle a page fault as opposed to a miss taking advantage of the greater time available.

Question 4

a) Draw a block diagram of a basic stored programme computer at the register level. Carefully label your diagram and explain the role of each of its main components in the machine code fetch / execute cycle.

(8 marks)

b) When a processor accesses RAM it may simply provide the address of the required memory location in what is called direct or absolute addressing mode. In all but the very simplest cases a range of different, less direct addressing modes is implemented.

i) Identify three such modes of indirect addressing and use your block computer diagram of part a) to illustrate how they would work.

ii) Explain why each of your chosen address modes might be included in support of the machine code instruction set of a typical computer.

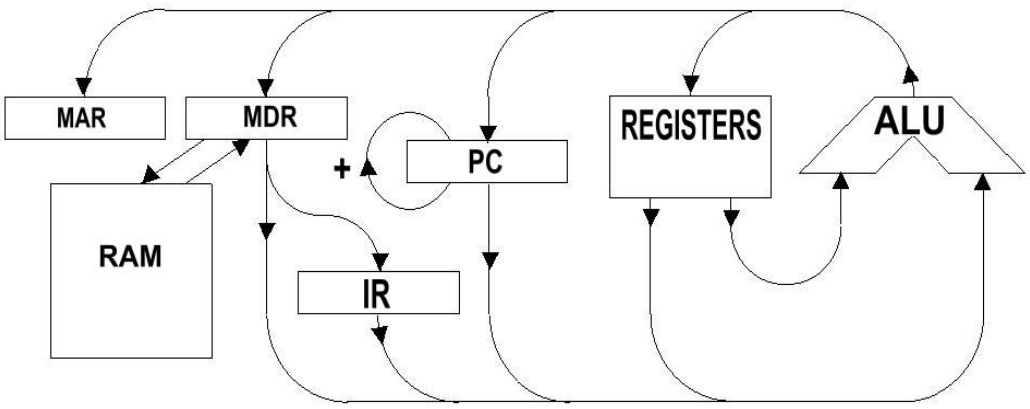
(10 marks)

c) Explain the principles of the strategy known as Direct Memory Access and discuss its significance as a feature of a digital computer.

(7 marks)

Answer Pointers

a) A block diagram of a computer should be drawn similar to the one shown below. A brief explanation of the role of each named item should be given. For example the PC holds the address of the next instruction to be fetched from memory and is incremented during each fetch phase.



b) There are many forms of indirect addressing and three of these should be selected. For example PC Relative addressing. In this case an offset value forms the operand of an instruction and this is added to the current value held in the Program Counter. In this way the instruction identifies data relative to the current PC value and means that code can be position-independent i.e. it can be run at any location in memory.

c) DMA is used to transfer data between main store and high speed devices such as hard disks. A second processor known as a Direct Memory Access Controller takes control of the system buses from the main system processor for the duration of a DMA operation. A system of handshakes is used to ensure there is no contention for the buses during the DMA operation. The request for transfer from the interface is passed forward by the DMAC to the main processor as a hold request. The main processor disconnects from the buses and acknowledges to the DMAC that it has relinquished control. The DMAC will already have received information about the size, direction and memory addresses for the transfer and now signals to the interface that transfer can start. Once the required number of bytes has been transferred the handshake signals are negated in turn and the main system processor regains control of the system.

The key feature of DMA is that the DMAC has internal microcode for the transfer process and does not require an external machine code program. Thus the full bus bandwidth can be devoted to transfer of data.

Examiner's Guidance Notes

While answers for a) were patchy, answers for b) and c) were complete as candidates well understood the topics of processor addressing and DMAC transfers of data.

Question 5

a) A computer is to be constructed from the list of components given in the table below. Calculate its reliability over 2000 hours. State clearly any assumptions you make in arriving at your answer

(14 marks)

component type	number in system	failure rate (% per 1000 hrs)
integrated circuits	25	0.0012
capacitors	52	0.019
resistors	27	0.006
Wire wraps	1424	0.00001

b) Discuss three strategies that can be used to improve the *reliability* of a computer system by using redundancy at the component and/or system level.

(11 marks)

Answer Pointers

a) Failure rate for the system is the sum of the failure rates for all the individual components in the system:
1.1942 % per 1000hours or $1.1942 * 10^{-5}$ failures per hour.
The reliability equation states that:

$R_t = e^{-\lambda t}$ where: λ is the system failure rate and t is the time.

Hence: R = 0.976 or 97.6 %

Assumes: Component failure rates are not a function of time.
A single failure brings down the system.
Component failures are independent of each other.

b) A variety of strategies could be discussed such as the hammock network for resistors at the component level and system level redundancy such as the triple mode redundant majority vote system.

Examiner's Guidance Notes
Very few attempted this question, and those who did were partially explain the failure rate, but got the reliability wrong. There were no sensible discussions on strategies for improving reliability of computer systems.

Question 6

a) Each new generation of computers based on the conventional von Neumann architecture is faster than the preceding one. This is in part due to advances in the fabrication technology of the integrated circuit components used to construct the machines. Discuss the assertion that "the physical laws governing the behaviour of circuit components and their interactions will soon limit further advances".

(7 marks)

b) Outline the principles of operation of either a Quantum Computer or a Neural Network and explain how your chosen design may overcome some of the physical limitations that you discussed in part a) of this question.

(18 marks)

Answer Pointers

a) The discussion of the limitations imposed by the known physical laws should address most of the topics listed below:
- velocity of light as the ultimate signal speed;
- storage of one bit per electron;
- heat dissipation – faster circuits, more heat;
- miniaturization – ability to draw finer detail;
- quantum tunnelling.

b) An outline discussion of the principles of operation of one of the novel computer architectures should be given together with a discussion of how it might mitigate some of the physical limitations discussed in the earlier part of the question.

Examiner's Guidance Notes
This question was the lowest in the order of candidates' priority, apart from a few feeble attempts to get some points together, the question was largely untouched.