Answer 3 Questions

The use of Electronic Calculators is not permitted in this examination.

Question 1

Why is cache memory needed and why does it work?. [6 Marks]

Discuss the provision of cache memory. [12 Marks]

A CPU running in a system with a clock frequency of 100MHz needs 10 clock cycles to access memory. It has a 64Kbyte cache with a memory access time of 20ns and a miss rate of 15%.
What is the average memory access time in nanoseconds? State any assumptions made.
[5 Marks]

This system is upgraded by adding a faster cache of 16Kbytes and 1 clock access time between the CPU and the 64Kbyte cache to give a 2-level cache hierarchy. In 10000 memory accesses, there are 3000 misses at the new primary cache and 1500 misses at the secondary cache.
What are the miss rates of

(a) the primary cache

(b) the secondary cache

(c) the combined cache

and what is the average memory access time in nanoseconds? [10 Marks]

End of Question 1

Question 2

(i) What is the role of the interface in performing Input and Output transfers. [3 Marks]

(ii) Explain the role of tri-state drivers and latches in input and output interfaces via block diagrams of simple examples of input and output interfaces, and explain the transfer of data between the CPU and each of these interfaces in terms of the instruction executed by the CPU, the activity on the system busses and actions at the interface. [12 Marks]

(iii) Explain the role and operation of status registers and flow control signals in parallel I/O interfaces. [8 Marks]

(iv) Discuss the use of polling, interrupts and DMA in performing I/O transfers. [10 Marks]

End of Question 2

Turn Over

Question 3

Answer 2 out of (a), (b) or (c)

a) i) Explain the meaning of the following sentence “The magnetic disk drive has 8 *surfaces*, 1000 *tracks* per surface, 50 *sectors* per track and 1Kbytes per sector”. [4 marks]

ii) Why are tracks divided into sectors? [4 marks]

iii) The disk in (i) has an average seek time of 10 ms and rotates at 6000 r.p.m. Estimate the average rotational latency and explain why it is beneficial to store all the data from a file in a single cylinder. [4 marks]

iv) A file occupies 40 sectors on the disk of (iii) and these sectors are randomly distributed over the disk. Calculate the time to read all the file.
The disk is re-organised so that sectors are allocated in blocks of 4 sequential sectors within a cylinder. How long does it now take to read the file, assuming blocks used are randomly distributed over the disk?
What are the possible disadvantages of this re-organisation? [4 marks]

(b) Why are interrupts useful and how does the interrupt system work? [8 Marks]

A CPU running at 50Mhz performs an instruction every 2 clock cycles on average.
On an interrupt, there is a hardware overhead of 8 clock cycles.
An interrupt service routine has been written that transfers one item of data to an output interface, and this routine has a 16 instruction overhead and requires 5 instructions to transfer the data item to the interface.
Calculate the maximum average data transfer frequency. [4 Marks]

The interface hardware can be replaced with an improved design that allows several data items to be buffered in the interface and for an interrupt to be generated when the interface buffer becomes empty. This allows several data items to be transferred to the interface for a single interrupt.
What is the minimum size of the interface buffer to achieve an average data rate of 4Mhz? [4 Marks]

Question 3 continued on next page

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Question 3 continued

(c) Many CPUs have a stack. What is the stack and why is it useful? Explain how it is accessed. [8 Marks]

A C compiler for a CPU with 32-bit addresses and registers maps integers, pointers and floats on to 4 bytes of memory and always saves 4 registers to the stack frame on a function call.

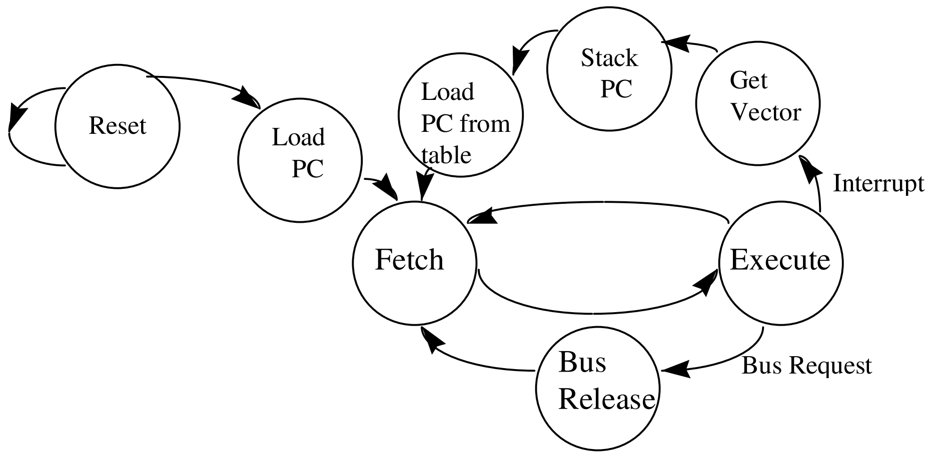
Draw a diagram of the stack frame created on a call to the function *insert_record* below and calculate the amount of memory occupied. [8 Marks]

```
struct record {
        struct record * next ;
        int reference ;
        int value ;
} ;
int insert_record(struct record * ptr, int ref, int val, int count) {
    struct record * np = ptr->next ;
    int   nr      =     np->reference;
        if (ref >reference) {
            return insert_record(np, ref, val, count++) ;
        } else {
            ptr->next = build_new_record(np, ref, value) ;
        }
        return count ;
}
struct record * build_new_record(struct record * p, int r, int v) {
    struct record * tp = (struct record *) malloc (sizeof(struct record)) ;
            tp->next = p ;
            tp->reference = r ;
            tp->value = v ;
            return tp ;
}
```

End of Question 3

Question 4

Below there is the state diagram for the control of a CPU.



Discuss the operation and activities of this CPU and its interaction with surrounding components in relation to this diagram. [15 Marks]

The datapath inside a modern CPU usually has a 3-bus architecture rather than a 1-bus or 2-bus architecture. Explain the use of these busses and explain why a 3-bus architecture is now used. [8 Marks]

A CPU with a 5-stage pipeline executes the instruction sequence shown below:-

load	0(r6), r3
add	r1, r2
sub	r2, r3
store	r3, 0(r6)

Draw a pipeline diagram showing the execution of the different stages of each of these instructions and where pipeline stalls occur.

Calculate the average number of clock cycles per instruction for this sequence assuming that a pipeline stage executes in one clock cycle. [8 Marks]

End of Question 4

Question 5

Write fully on **3** of the following:-

i) Handling text in computers. [11 Marks]

ii) Compiled, Semi-Compiled and Interpreted code. [11 Marks]

iii) The role and implementation of a Micro-Programmed Control Unit. [11 Marks]

iv) The role of an Operating System and the operation of its scheduler in a multi-process system. [11 Marks]

End of Paper

v) Floating point numbers and the IEEE standard. [11 Marks]

End of Paper