Answer QUESTION ONE and TWO other questions.

1.

a) What is the difference between **digital** and **analog** data representations? Why is it usually preferable to store and transmit data in digital form? Given that a digital system is to be used, why would the 2-digit binary system normally be preferable to the 10-digit decimal one?

[9 marks]

b)

(i) Define each of the following terms:-

(1) assembler
(2) cache
(3) central processor unit
(4) memory
(5) instruction set architecture

[10 marks]

(ii) Draw a diagram of the main functional components of a computer system. Your diagram should include any necessary communications lines. Use this diagram to briefly explain the fetch and execute cycle of a computer as it executes a program.

[5 marks]

c) Explain the differences between the types of semiconductor memory used for storage in the computer's main read/write memory and in cache memory.

[9 marks]

TURN OVER

2.

a) Define the meaning of the condition code flags C, Z, N and V (**C**arry, **Z**ero, sig**N** and o**V**erflow). In each case state clearly the conditions under which that flag would be set to 1.

[8 marks]

b)

(i) What are the largest (most positive) and smallest (most negative) decimal integers that could be represented using 8-bit 2's complement notation?

[2 marks]

(ii) Perform the addition $51_{10} + 83_{10}$ using 8-bit 2's complement arithmetic. What is the decimal value of the result? What would be the values of the flags C, Z, N and V after this addition had been performed?

[4 marks]

c) Explain the difference between

(i) active-high and active-low signals

(ii) positive and negative logic

[4 marks]

d) A circuit has four inputs a, b, c, d representing 4-bit binary numbers 0000 (0_{10}) to 1111 (15_{10}). 'a' is the most significant bit, 'd' is the least. The circuit has one output y which is true if and only if the number represented by the input is prime (note that zero (0000) and one (0001) are not considered to be prime numbers).

(i) Write out a truth table for this circuit, and hence obtain an expression in **sum of products** form for y in terms of a, b, c, d. (Assume that positive logic is to be used.)

[4 marks]

(ii) Simplify the expression obtained in (i) using the **Karnaugh map** technique to show that it can be reduced to the form

$$y = b.\overline{c}.d + \overline{a}.b.d + \overline{b}.c.d + \overline{a}.\overline{b}.c$$

[4 marks]

(iii) Implement the above expression as a combinatorial logic circuit using **NAND gates only**. (Hint: what is the effect of taking the complement of both sides of the above twice in succession?)

[7 marks]

CONTINUED

3.

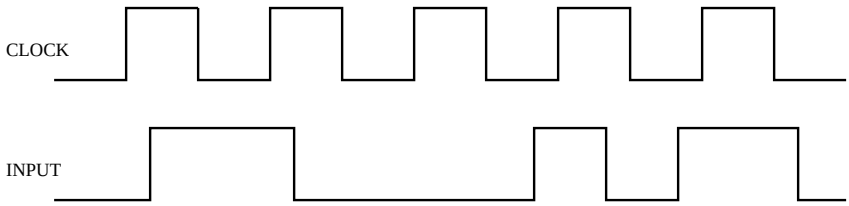
a) Explain the difference between **combinatorial** and **sequential** digital circuits. In which parts of a computer system are these types of circuitry typically used, and for what functions?

[7 marks]

b) Why can the use of **level triggered** flip-flops lead to problems in sequential logic circuits? How does the use of **edge triggering** overcome these difficulties?

[8 marks]

c) Consider the clock and input waveforms below.



Provide a timing diagram for the Q output of a D flip-flop. Assume that the flip-flop is

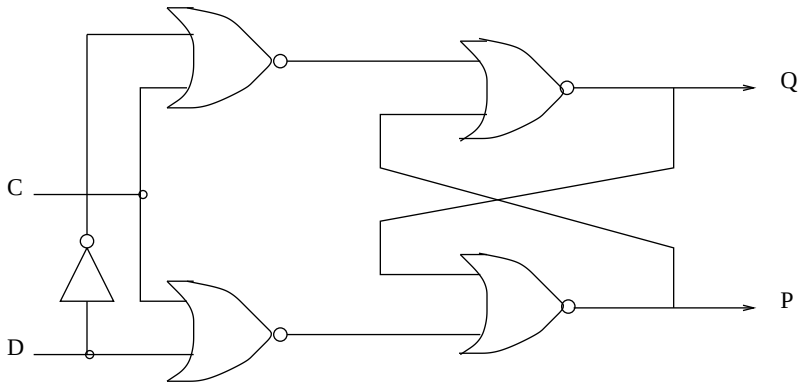
(i) level sensitive
(ii) rising edge triggered
(iii) falling edge triggered

[6 marks]

[Qu.3 cont. over page]

[Qu.3 continued]

d) Consider the sequential circuit below



Assuming that at t = 0 P = 1 and Q = 0, copy and complete the table below by calculating the values of the outputs P and Q at each of the times t = 2..9, using in each case the tabulated input values C and D at time t, and the values of P and Q at t-1. (Remember that the output of a NOR gate is 1 if and only if both inputs are 0.)

Time	**C**	**D**	**P**	**Q**
0	-	-	1	0
1	1	1	1	0
2	1	0		
3	0	0		
4	1	1		
5	0	1		
6	1	1		
7	0	1		
8	0	0		
9	1	0		

[12 marks]