Model Answers for E4.16

Question 1 (40%)

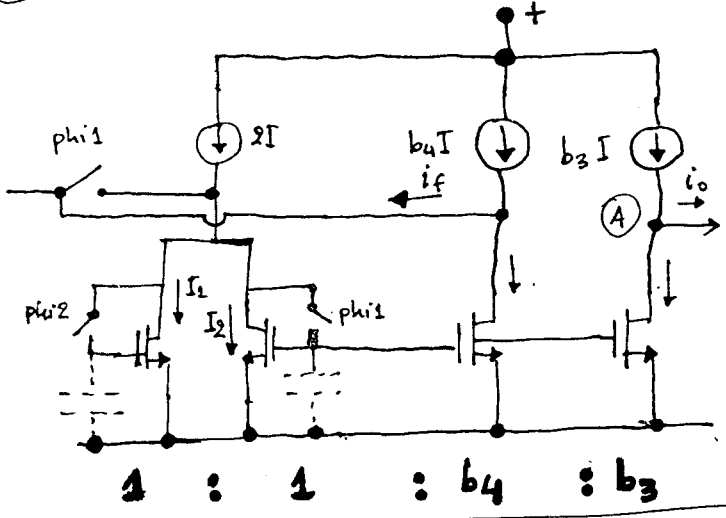
(a) [Bookwork] Current-Mode Analogue Sig. Proc. [20%]

→ The switched-capacitor (SC) technique requires linear floating capacitors; these can be implemented as poly-poly structures but the cost of such processes is high. Cheap digital processes do not offer two layers of polysilicon. For the switched-current (SI) technique we do not need linear capacitors; the memory action can be performed by means of the non-linear C_{gs} capacitor of a MOS device.

→ SC circuits use op-amps; SI circuits do not need op-amps (less complex designs)

→ The trend towards low power-supply levels means that it is difficult to achieve high-speed and increased dynamic range SC designs since it is difficult to have low-voltage, high-speed op-amps. SI circuits operate in current-mode, voltage swings are smaller (mitigating the reduction of the power supply voltage) allowing low power-supply voltage operation and have the potential for high-speed and low-power operation. Hence, the SI technique is an analogue technique for digital technology.

(b) [New exercise based on taught theory]



During $phi_2 (n-1)$:

$$I_1(n-1) + I_2(n-1) = 2I$$

From KCL at node **A**:

$$b_3 I_2(n-1) + i_o(n-1) = b_3 I \Rightarrow$$

$$\Rightarrow I_2(n-1) = I - \frac{i_o(n-1)}{b_3} \Rightarrow I_1(n-1) = I + \frac{i_o(n-1)}{b_3}$$

During $\phi_{1}(n)$:

$$I_1(n) + I_2(n) = i_{in}(n) + 2I + i_f$$

$$i_f = b_4 I - b_4 I_2(n)$$

from KCL at (A) $\rightarrow$ $b_3 I_2(n) + i_o(n) = b_3 I \Rightarrow$

$$\Rightarrow I_2(n) = I - \frac{i_o(n)}{b_3}$$

$$\Rightarrow i_f = \left[\frac{b_4}{b_3}\right] i_o(n) \Rightarrow$$

$$\Rightarrow \quad I_1(n) + I_2(n) = i_{in}(n) + 2I + i_f$$

$$i_f = \left[\frac{b_4}{b_3}\right] i_o(n)$$

$$I_2(n) = I - \frac{i_o(n)}{b_3}$$

$$I_1(n) = (\text{due to memory action}) = I_1(n-1) = I + \frac{i_o(n-1)}{b_3} \Rightarrow$$

$$\cancel{I} + \frac{i_o(n-1)}{b_3} + \cancel{I} - \frac{i_o(n)}{b_3} = i_{in}(n) + \cancel{2I} + \frac{b_4}{b_3} i_o(n) \Rightarrow$$

$$\Rightarrow \quad i_o(n-1) - i_o(n) = b_3 i_{in}(n) + b_4 i_o(n) \Rightarrow$$

$$\Rightarrow \quad z^{-1} i_o(z) - i_o(z) = b_3 i_{in}(z) + b_4 i_o(z) \Rightarrow$$

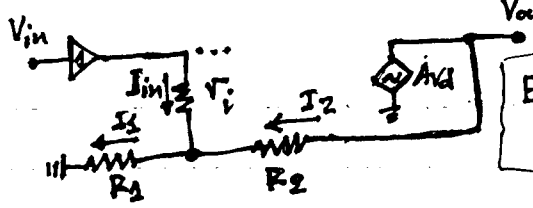
$$\Rightarrow H(z) = \frac{i_o(z)}{i_{in}(z)} = \frac{-b_3}{(1+b_4) - z^{-1}} = -\frac{\frac{b_3}{1+b_4}}{1 - \frac{z^{-1}}{1+b_4}}$$

inverting damped integrator

for $z = e^{sT} = e^{j\omega T} \Rightarrow z^{-1} \simeq 1 - j\omega T$ when $\omega T \ll 1 \Rightarrow$

$$H(j\omega) \simeq -\frac{b_3}{\cancel{1}+b_4-\cancel{1}+j\omega T} = -\frac{\left(b_3/b_4\right)}{1 + j\omega\left(\frac{T}{b_4}\right)} \Rightarrow$$

$\Rightarrow$ time constant $= T/b_4$ (& dc-gain $= b_3/b_4$)



Question 2

[BookworK]

(a) KVL → $I_1 R_1 + I_2 R_2 = V_{out}$; KCL → $I_2 = I_1 - I_{in}$ } $\Rightarrow$ $(R_1+R_2) I_1 - R_2 I_{in} = V_{out}$ $\Rightarrow$

$$\Rightarrow \quad I_1 = \frac{V_{out}}{R_1+R_2} + \frac{R_2}{R_1+R_2} I_{in}$$

$$\text{Hence, } I_2 = \frac{V_{out}}{R_1+R_2} - \frac{R_1}{R_1+R_2} I_{in}$$

$$\text{But} \quad V_{in}^{/} - I_1^{/} R_1 = I_{in} r_i \quad \Rightarrow$$

($V_{in}^{/} \rightarrow V_+$, $I_1^{/} \rightarrow V_-$)

$$V_{in} - \frac{R_1}{R_1+R_2} V_{out} - \frac{R_1 R_2}{R_1+R_2} I_{in} = I_{in} r_i \quad \Rightarrow$$

$$\Rightarrow \quad I_{in} = \frac{V_{in} - \frac{R_1}{R_1+R_2} V_{out}}{r_i + \frac{R_1 R_2}{R_1+R_2}} = \frac{(R_1+R_2) V_{in} - R_1 V_{out}}{r_i (R_1+R_2) + R_1 R_2}$$

$$\text{Hence} \quad V_{out} = A I_{in} r_i = \frac{A(R_1+R_2) r_i V_{in} - A r_i R_1 V_{out}}{r_i (R_1+R_2) + R_1 R_2} \Rightarrow$$

$$\Rightarrow \quad \frac{V_{out}}{V_{in}} = \frac{\frac{A(R_1+R_2) r_i}{r_i (R_1+R_2) + R_1 R_2}}{\frac{r_i (R_1+R_2) + R_1 R_2 + A r_i R_1}{r_i (R_1+R_2) + R_1 R_2}} = \frac{A(R_1+R_2) r_i}{r_i (R_1+R_2) + R_1 R_2 + A r_i R_1} =$$

$$\Rightarrow \quad \frac{V_{out}}{V_{in}} = \left(1 + \frac{R_2}{R_1}\right) \frac{A r_i}{r_i \left(1 + \frac{R_2}{R_1}\right) + R_2 + A r_i} \Rightarrow$$

$$\Rightarrow \quad \text{(setting } 1 + \tfrac{R_2}{R_1} = G\text{)} \quad \frac{V_{out}}{V_{in}} = G \frac{A}{A + G + R_2/r_i}$$

for the CFOA, $R_2/r_i \gg G \Rightarrow \frac{V_{out}}{V_{in}} \simeq \frac{G A}{A + R_2/r_i}$

Assuming α dependence $A = \frac{A_0}{1+j f/f_0}$

$$\frac{V_{out}}{V_{in}} = \frac{G \frac{A_0}{1+jf/f_0}}{\frac{A_0}{1+jf/f_0} + R_2/r_i} = \frac{G A_0}{A_0 + R_2/r_i} \frac{1}{1 + j \frac{f \cdot R_2}{f_0} \frac{1}{r_i} \frac{1}{A_0 + R_2/r_i}} \Rightarrow$$

$$\Rightarrow \frac{V_{out}}{V_{in}} \overset{(A_0 \gg R_2/r_i)}{\simeq} G \frac{1}{1 + j \frac{f}{\left[\frac{A_0 f_0 r_i}{R_2}\right]}}$$

Hence gain $= 1 + R_2/R_1$

whereas bandwidth $= \frac{A_0 f_0 r_i}{R_2}$.

Setting R_2 we set the bandwidth and setting R_1 we set the gain for the determined bandwidth.

[BOOKWORK]

(b) $V_{out} = A I_{in} r_i = [A r_i] I_{in} = Z_t I_{in} \Rightarrow$

$\Rightarrow$ V_{out} can be considered as the output of a transimpedance amplifier of gain $Z_t = A r_i$

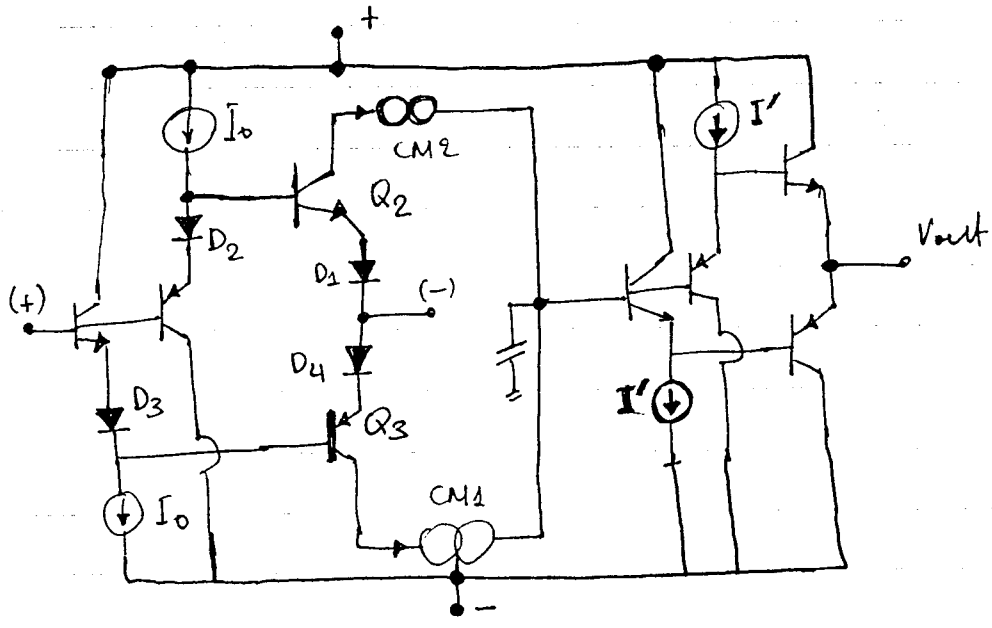
Hence, $\frac{V_{out}}{V_{in}} \simeq \frac{A G}{A + R_2/r_i} = \frac{(A r_i) G}{(A r_i) + R_2} = G \frac{Z_t}{Z_t + R_2}$

When $Z_t = R_0 // \frac{1}{jC_0\omega} = \frac{R_0}{1+j f/f_0}$ with $R_0 C_0 = \frac{1}{2\pi f_0}$

$$\frac{V_{out}}{V_{in}} = G \frac{R_0}{R_0 + R_2} \frac{1}{1 + j \frac{f}{\frac{f_0 (R_0 + R_2)}{R_2}}}$$

bandwidth

(c)



Reduced offset voltage can be achieved by including the diodes (diode-connected BJT devices) D_1, D_2, D_3 & D_4. When

D_1 is implemented with p-type BJT

D_2 -"- -"- -"- n-type BJT

D_3 -"- -"- -"- p-type BJT

and D_4 -"- -"- -"- n-type BJT

then $V_+ - V_- \simeq 0$ because from (+) terminal to (-) we meet two n-type base-emitter junctions & two p-type base-emitter junctions => matching. However, the small signal offset at the (-) terminal increases because the output resistance at the (-) terminal increases: $R_- = (r_{e_2} + r_{D_1}) // (r_{e_3} + r_{D_4})$. Hence voltage offset is reduced but the r_i value of the **CFOA** is increased and the amplifier becomes more susceptible to "bandwidth roll-off with gain" for given values of R_1, R_2.

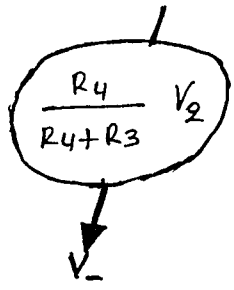
Question 3

[Bookwork]

(a) (i) $V_+ = \frac{R_4}{R_4+R_3} V_2$

$V_- = V_+ \Rightarrow$ current through $R_1 = \dfrac{V_1 - \frac{R_4}{R_4+R_3} V_2}{R_1}$

Hence, $V_{out} = \left(\frac{R_4}{R_4+R_3} V_2\right) - \left[\dfrac{V_1 - \frac{R_4}{R_4+R_3} V_2}{R_1}\right] R_2 \Rightarrow$



$\Rightarrow V_{out} = -\left(\frac{R_2}{R_1}\right) V_1 + \left(1 + \frac{R_2}{R_1}\right) \frac{R_4}{R_4+R_3} V_2 \Rightarrow$

$\Rightarrow V_{out} = K_2 V_2 - K_1 V_1$

In order to have a difference amplifier the following condition should hold:

$$\left(1 + \frac{R_2}{R_1}\right) \frac{R_4}{R_4+R_3} = \frac{R_2}{R_1} \Rightarrow$$

$$\Rightarrow \frac{1 + R_2/R_1}{1 + R_3/R_4} = \frac{R_2}{R_1} \Rightarrow$$

$$\Rightarrow \boxed{\frac{R_2}{R_1} = \frac{R_4}{R_3}} \leftarrow \text{condition for difference amplifier.}$$

For practical reasons (minimise output offset due to input bias current) it is better if $R_2 = R_4$ & $R_1 = R_3$.

(ii) Common-mode only

$$V_2 = V_1 \Rightarrow \begin{bmatrix} V_{diff} = V_2 - V_1 = 0 \\ V_c = \frac{V_1+V_2}{2} = V_1 \end{bmatrix} \Rightarrow V_{out} = (K_2 - K_1)\, V_1 \Rightarrow$$

$$\boxed{A_c = K_2 - K_1}$$

↑ common-mode gain

Differential-mode only

$$\left.\begin{aligned} V_2 &= V_d/2 \\ V_1 &= -V_d/2 \end{aligned}\right\} \Rightarrow \begin{bmatrix} V_{diff} = V_d \\ V_c = \frac{V_1+V_2}{2} = 0 \end{bmatrix} \Rightarrow V_{out} = \frac{K_2+K_1}{2} V_d \Rightarrow$$

$$\Rightarrow \boxed{A_d = \frac{K_2+K_1}{2}}$$

↑ differential gain

Hence $CMRR = \frac{A_d}{A_c} = \frac{1}{2} \frac{K_2+K_1}{K_2-K_1}$

$$K_2 + K_1 = \frac{1+\frac{R_2}{R_1}}{1+\frac{R_3}{R_4}} + \frac{R_2}{R_1} = \frac{R_1R_4 + 2R_4R_2 + R_2R_3}{R_1R_3 + R_1R_4}$$

$$K_2 - K_1 = \frac{1+\frac{R_2}{R_1}}{1+\frac{R_3}{R_4}} - \frac{R_2}{R_1} = \frac{R_4R_1 - R_2R_3}{R_1R_3 + R_1R_4}$$

$\Rightarrow$

$$\Rightarrow \quad CMRR = \frac{1}{2} \frac{R_1R_4 + 2R_4R_2 + R_2R_3}{R_4R_1 - R_2R_3} \Rightarrow$$

$\Rightarrow$ CMRR infinite when

$$\frac{R_4}{R_3} = \frac{R_2}{R_1}$$ which is the same condition for the op-amp to implement as difference amplifier.

A high CMRR value depends strongly upon resistor matching. Due to the finite tolerances of the resistors the CMRR will drop significantly. Resistor of very low tolerance ($\pm 0.1\%$) and temperature coefficient cost.

[Bookwork]

(5) The circuit depicts a current-mode instrumentation amplifier.

Differential-mode :

The circuit operation is based on the supply-current sensing technique. When $V_1 > V_2$ a current $I = \frac{V_1 - V_2}{R_1}$ is drawn from

OA1 (from its +ve power supply when its output stage operates in class B) and through the action of the current mirors CM1 & CM2 is reflected/recreated at the -ve input terminal of OA3 giving $V_{out} = \frac{R_2}{R_1}(V_1 - V_2)$. When $V_2 > V_1$ then a current $I = \frac{V_2 - V_1}{R_1}$ is fed into the output of OA1 (into its -ve power supply when its output stage operates in class B) and is again reflected/recreated at at the -ve input terminal of OA3.

Common-mode : When $V_1 = V_2$ then $I = 0 \Rightarrow V_{out} = 0$.

The main advantage of this instrumentation amplifier is that it achieves a high CMRR value without the need for precise matched resistors (case for the traditional 3-op-amp instrumentation amplifier). Simplicity and wider bandwidth is a secondary advantage.

The gain accuracy is limited by the accuracy of the current-mirors; if 1 is the current transfer of the current mirors then $V_{out} = 1 \frac{R_2}{R_1}(V_1 - V_2)$. The CMRR performance is mainly limited by gain bandwidth (GB) product mismatching between OA_1 & OA_2; it can be shown that the common-mode gain $\sim (GB_{OA1} - GB_{OA2})$.

Question 4

[BookWork]

(a) Assumptions & conditions:

equal number of CW & ACW npn junctions

—"— —"— —"— —"— —"— pnp —"—

Same V_T (i.e. temperature) for all devices

All npn (pnp) devices have same current density J_{sn} (J_{sp})

When the above hold:

$$\text{CW} \sum_{j=1}^{m} V_{be_j} = \text{ACW} \sum_{j=1}^{m} V_{be_j} \Rightarrow$$

$$\Rightarrow \text{CW} \sum_{j=1}^{m} V_T \ln\left[\frac{I_{C_j}}{J_{S_j} A_j}\right] = \text{ACW} \sum_{j=1}^{m} V_T \ln\left[\frac{I_{C_j}}{J_{S_j} A_j}\right] \Rightarrow$$

$$\Rightarrow \text{CW} \prod_{j=1}^{m} \left[\frac{I_{C_j}}{J_{S_j} A_j}\right] = \text{ACW} \prod_{j=1}^{m} \left[\frac{I_{C_j}}{J_{S_j} A_j}\right] \Rightarrow$$

$$\Rightarrow \text{CW} \prod_{j=1}^{m} \left[\frac{I_{C_j}}{A_j}\right] = \text{ACW}\left[\prod_{j=1}^{m} \frac{I_{C_j}}{A_j}\right]$$

BIPOLAR TRANSLINER PRINCIPLE

[BookWork]

MOS TRANSLINER PRINCIPLE:

$$\text{CW} \sum_{j=1}^{m} \sqrt{\frac{I_{D_j}}{K_j}} = \text{ACW} \sum_{j=1}^{m} \sqrt{\frac{I_{D_j}}{K_j}}$$

$$K_j = \frac{\mu C_{ox}}{2} \frac{W}{L}$$

Question shortened by the 2nd marker →

Disadvantages:

— "Sum of roots" is not as widely useful as bipolar "product"

— MOS square law holds over a smaller current range than the bipolar exponential law

— process parameters do not cancel

automatically for "mixed" (NMOS & PMOS) TL loops.

Advantage: MOS TL circuits do not suffer from beta errors

(b) [New exercise based on taught theory]

Applying the TLP:

(i) $$\left[\frac{I-I_x}{2}\right]^2 I_4 = I_3 \left[\frac{I+I_x}{2}\right]^2 \Rightarrow$$

$$\left.\begin{aligned} \frac{I_4}{I_3} &= \left[\frac{I+I_x}{I-I_x}\right]^2 \\ \text{But also (KCL)}\quad I_3 + I_4 &= I \end{aligned}\right\} \Rightarrow \quad I_4 = \frac{I\,(I+I_x)^2}{(I-I_x)^2+(I+I_x)^2}$$

$$I_3 = \frac{I\,(I-I_x)^2}{(I-I_x)^2+(I+I_x)^2}$$

(ii) $$\left.\begin{aligned} I_2 &= \frac{I-I_x}{2} + \frac{I\,(I+I_x)^2}{(I-I_x)^2+(I+I_x)^2} \\ I_1 &= \frac{I+I_x}{2} + \frac{I\,(I-I_x)^2}{(I-I_x)^2+(I+I_x)^2} \end{aligned}\right\} \Rightarrow$$

$$I_2 - I_1 = -I_x + \frac{4I^2 I_x}{2(I^2+I_x^2)} \Rightarrow$$

$$I_2 - I_1 = \frac{-I_x 2I^2 - I_x 2I_x^2 + 4I^2 I_x}{2(I^2+I_x^2)} \Rightarrow$$

$$I_2 - I_1 = \frac{I^2 I_x - I_x^3}{I^2+I_x^2}$$

When $I_x = y\,I$, then $I_2 - I_1 = I\,\dfrac{y-y^3}{1+y^2}$

[New exercise based on taught theory]

(c) (i) Applying the TLP & KCL yields:

$$(2I + I_x + I_2)\,I = (I+I_x)\,(0.92I + I_2) \Rightarrow$$

$$\Rightarrow \quad I_2 = \frac{(2I+I_x+I_2)\,I}{I+I_x} - 0.92I$$

(ii) $$(I+I_x)\,[3I-(I+I_x)] = \frac{2/3\,I}{A}\,\frac{\frac{(2I+I_x+I_z)\,I}{I+I_x} - 0.92\,I}{A} \rightarrow$$

$$\Rightarrow \quad \frac{A^2\,(I+I_x)(2I-I_x)}{[2/3]\,I} + 0.92\,I = \frac{(2I+I_x+I_z)\,I}{I+I_x} \Rightarrow$$

$$\Rightarrow \quad \left(\frac{3A^2\,(I+I_x)(2I-I_x)}{2I} + 0.92\,I\right)\frac{I+I_x}{I} = 2I+I_x+I_z \Rightarrow$$

$$\Rightarrow \quad I_z = \left(\frac{3A^2(I+I_x)(2I-I_x)}{2I} + 0.92\,I\right)\frac{I+I_x}{I} - 2I - I_x$$

(iii) $$I_z = \frac{\left\{3A^2\,(2I^2+II_x-I_x^2)+1.84\,I^2\right\}(I+I_x) - 4I^3 - 2I^2 I_x}{2I^2} \rightarrow$$

$$\mathbf{I_z = (3A^2-1.08)\,I + \left(\frac{3A^2-0.16}{2}\right) I_x - \frac{3A^2}{2}\,\frac{I_x^3}{I^2}}$$

When $\frac{3A^2}{2} = 0.54 \Rightarrow A = 0.6$ then

indeed $$\mathbf{I_z = 1.54\,I_x - 0.54\,\frac{I_x^3}{I^2}}$$

Question 5

[New exercise based on taught theory]

(a) from the given state-space relations:

$$\left.\begin{aligned} \left[s + \frac{\omega_o}{Q}\right] X_1(s) - \omega_o X_2(s) &= 0 \\ \omega_o X_1(s) + s X_2(s) &= \omega_o V(s) \end{aligned}\right\} \Rightarrow$$

$$D_{X_1} = \begin{vmatrix} 0 & -\omega_o \\ \omega_o V(s) & s \end{vmatrix} = \omega_o^2 V(s), \quad D_{X_2} = \begin{vmatrix} s+\omega_o/Q & 0 \\ \omega_o & \omega_o V(s) \end{vmatrix} = \omega_o \left(s + \frac{\omega_o}{Q}\right) V(s)$$

$$D = \begin{vmatrix} s + \frac{\omega_o}{Q} & -\omega_o \\ \omega_o & s \end{vmatrix} = s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2$$

Hence, $\dfrac{Y_1(s)}{V(s)} = \dfrac{X_1(s)}{V(s)} = \dfrac{\omega_o^2}{s^2 + (\omega_o/Q)s + \omega_o^2}$, Lowpass response

$$\frac{Y_2(s)}{V(s)} = \frac{X_2(s)}{V(s)} = \frac{\omega_o\left(s + \frac{\omega_o}{Q}\right)}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2}, \text{ "two-pole one-zero" respon}$$

(b)

$$x_1 = I_o e^{V_1/V_T} \Rightarrow \dot{x}_1 = x_1 \frac{\dot{V}_1}{V_T}$$

$$x_2 = I_o e^{V_2/V_T} \Rightarrow \dot{x}_2 = x_2 \frac{\dot{V}_2}{V_T}$$

Hence:

$$\left.\begin{aligned} x_1 \frac{\dot{V}_1}{V_T} &= -\left(\frac{\omega_o}{Q}\right)x_1 + \omega_o x_2 \\ x_2 \frac{\dot{V}_2}{V_T} &= -\omega_o x_1 + \omega_o u \end{aligned}\right\} \Rightarrow$$

$$C\dot{V}_1 = -\frac{(\omega_o C V_T)}{Q} + (\omega_o C V_T)\, e^{\frac{V_2 - V_1}{V_T}}$$

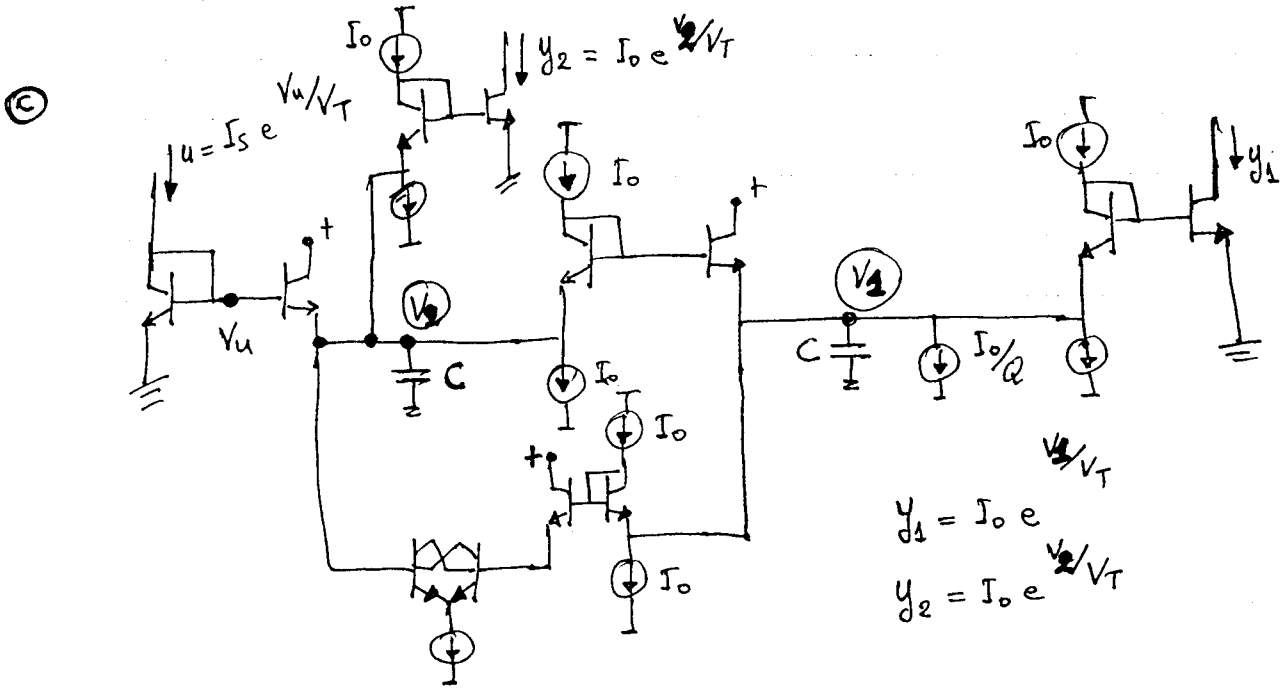
$$C\dot{V}_2 = -(\omega_o C V_T)\, e^{\frac{V_1 - V_2}{V_T}} + (\omega_o C V_T)\frac{I_s}{I_o} e^{\frac{V_u - V_2}{V_T}}$$

Setting $\omega_o C V_T = I_o$ = biasing current $\Rightarrow$

$$C\dot{V}_1 + I_o/Q = I_o\, e^{\frac{V_2 - V_1}{V_T}}$$

$$C\dot{V}_2 + I_o\, e^{\frac{V_1 - V_2}{V_T}} = I_s\, e^{\frac{V_u - V_2}{V_T}}$$

Non-linear log-domain design equations which can be interpreted as KCL relations involving capacitor currents, constant current sources & bipolar transistor collector currents operating according to their non-linear (exponential) V-I characteristic.



The above topology satisfies the non-linear design equations.

$$\omega_o C V_T = I_o \Rightarrow$$

$$\Rightarrow \quad I_o = (2\pi \times 4\times 10^6) \cdot 20\times 10^{-12} \times 0.026 \Rightarrow$$

$$\Rightarrow \quad I_o \simeq 13\,\mu A$$

Question 6

[Bookwork]

(a) Two N-port networks A & B must satisfy the following relation in order to be adjoint:

$$\sum_{n=1}^{N} \left(V_{An} I_{Bn} - V_{Bn} I_{An} \right) = 0$$

with V_{An} denoting the voltage of the n-th port of network A, etc....

(i) Resistor

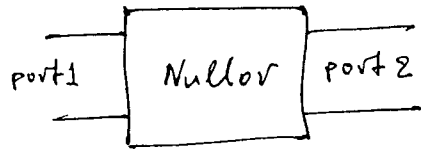
$V_A := R_A I_A$, one port

$$V_A I_B - V_B I_A = 0 \Rightarrow \frac{V_B}{I_B} = \frac{V_A}{I_A} \Rightarrow$$

But $\frac{V_A}{I_A} = R_A$

$V_B = I_B \cdot R_A$ (i.e. R_B), Hence the adjoint network of a resistor is a resistor of the same value.

(ii)



$V_A = [V_{A1} \; V_{A2}] = [0 \quad X]$

$I_A = [I_{A1} \; I_{A2}] = [0 \quad X]$

✗ denotes "any value"

Hence I want: $V_{A1} I_{B1} - V_{B1} I_{A1} + V_{A2} I_{B2} - V_{B2} I_{A2} = 0$

(V_{A1}: 0, I_{A1}: 0, V_{A2}: X, I_{A2}: X)

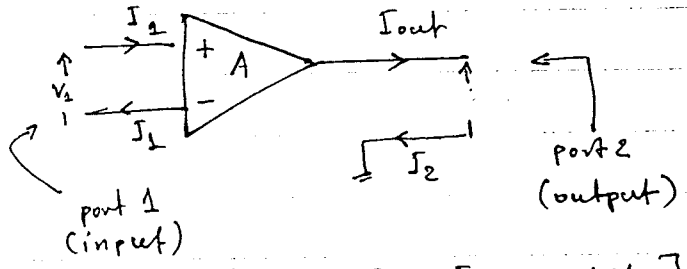
Hence when $V_B = [V_{B1} \; V_{B2}] = [X \quad 0]$

and $I_B = [I_{B1} \; I_{B2}] = [X \quad 0]$

the relation is satisfied.

Thus, the adjoint network of a nullor is another nullor with its input & output ports interchanged

(iii) voltage amplifier



$$V_A = [V_{A_1}\ V_{A_2}] = [V_{in}\ \ AV_{in}]$$

$$I_A = [I_{A_1}\ I_{A_2}] = [0\ \ \times]$$

Hence $V_{A_1} I_{B_1} - V_{B_1} I_{A_1} + V_{A_2} I_{B_2} - V_{B_2} I_{A_2} = 0$

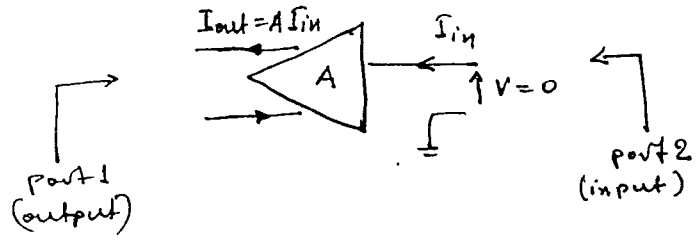
($V_{A_1} = V_{in}$, $I_{A_1} = 0$, $V_{A_2} = AV_{in}$, $I_{A_2} = \times$)

and when $V_B = [V_{B_1}\ V_{B_2}] = [\times\ \ 0]$

$I_B = [I_{B_1}\ I_{B_2}] = [-AI_{in}\ \ I_{in}]$

then the relation is satisfied

Thus, the adjoint network of an ideal voltage amplifier is a current amplifier with input and output ports interchanged:

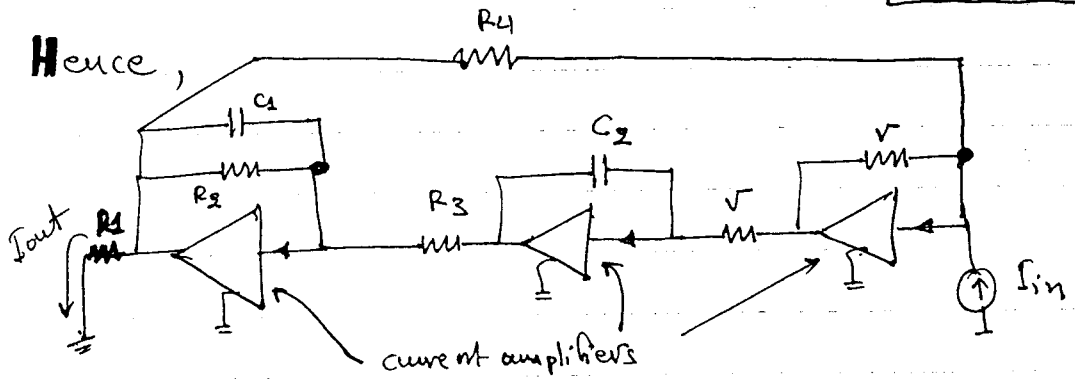


[New exercise based on taught theory]

(b) To find its current-mode equivalent we only need to find its adjoint bearing in mind that

R	is transformed to	R
C	—11—	C
& a voltage amplifier	—11—	to a current amplifier with its input & output ports interchanged

Hence,



high-gain [BookwoRK]

(c) (i) if "ideal amplifiers" are available, it doesn't matter what kind of amplifier you use

(ii) If practical amplifiers are available then for an I-I converter we should use a current-amplifier (CCCS) because with this choice the closed-loop bandwidth becomes independent of the source & load impedance levels. The price paid for this ~~is~~ cause is that the I-I converter bandwidth cannot be set independently of its gain (gain-bandwidth conflict).

(iii) When high performance CFs & VFs are available then we should choose any other amplifier except from a current amplifier. For, if we choose a

buffered transresistance amplifier (CCVS)
or a —||— transconductance —||— (VCCS)
or a —||— voltage amplifier (VCVS)

then the closed loop bandwidth of the converter can be set independently from the closed-loop gain.

(d) [New Combinatorial exercise based on tourniquet theory]

(i) $V_{cap} + V_T \ln\left(\frac{I_o}{I_s}\right) = V_T \ln\left(\frac{I_{out1}}{I_s}\right) \Rightarrow$

$$i_{cap} = C\dot{V}_{cap} = CV_T \frac{\dot{I}_{out1}}{I_{out1}}$$

(ii) Applying TLP:

$$u\,(2I_{out1}) = (4I_{out1}) \cdot I_d \Rightarrow$$

(u: due to p-type current mirror; $4I_{out1}$: due to p- & the n-type current mirrors)

$$\Rightarrow \quad u = 2I_d$$

(iii) Applying TLP:

$$I_{in} I_o = \left(2I_d + CV_T \frac{\dot{I}_{out1}}{I_{out1}}\right) I_{out1} \Rightarrow$$

($2I_d = u$)

$$I_{in} I_o = (2I_d) I_{out1} + CV_T \dot{I}_{out1} \Rightarrow$$

$$\Rightarrow \frac{I_{out1}(s)}{I_{in}(s)} = \frac{(I_o/CV_T)}{s + \left(\frac{2I_d}{CV_T}\right)}$$

However, $I_{out2} = 3 I_{out1} \Rightarrow$

$$\frac{I_{out2}(s)}{I_{in}(s)} = \frac{\frac{3I_o}{CV_T}}{s + \left(\frac{2I_d}{CV_T}\right)}$$

$s \to 0 \to$ gain $= \frac{3I_o/CV_T}{2I_d/CV_T} = \frac{3}{2}\frac{I_o}{I_d} = 1 \Rightarrow I_o = \frac{2I_d}{3} = \frac{20}{3}\,\mu A$

$$\omega_o = \frac{2I_d}{CV_T} \Rightarrow C = \frac{2I_d}{\omega_o V_T} = \frac{2\times 10\times 10^{-6}}{2\pi\times 1\times 10^6 \times 0.026} \approx 122\,pF$$