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AO5

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2004

MSc and EEE PART IV: MEng and ACGI

CURRENT-MODE ANALOGUE SIGNAL PROCESSING

Wednesday, 12 May 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks

Corrected Copy

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : E. Drakakis
Second Marker(s) : C. Papavassiliou

1.

a. Design a unit delay switched current cell of current gain N, both for positive and negative N. What is the maximum signal frequency on which this cell can operate?

[8]

b. Design a switched current Infinite Impulse Response filter implementing the following transfer function:

$\frac{i_o}{i_i} = \frac{z-1}{z+1}$, at a sampling rate of 1kHz. Specify the clock frequency.

[7]

c. Discuss 3 limitations of switched current cells, and propose solutions that alleviate these limitations. Draw relevant diagrams.

[5]

2.

a. Draw a diagram for the standard 3 op-amp instrumentation amplifier, and describe its operation and advantages over a single op-amp difference amplifier.

[4]

b. Draw a diagram for a current mode instrumentation amplifier. What advantages does it have over the voltage mode instrumentation amplifier?

[4]

c. Describe the current feedback op-amp, and draw a transistor level diagram of a commercial current feedback op-amp. Explain why a current feedback op-amp has a theoretically infinite slew rate.

[6]

d. Draw circuit diagrams to show if and how a current feedback op-amp can be used to implement:

   i. An inverting voltage amplifier of gain 10

   ii. A non inverting voltage amplifier of gain 6

   iii. A low pass filter with a pole at zero frequency.

[6]

3.

a. Describe the current conveyor. How does a second generation current conveyor differ from a first generation current conveyor? How does a current conveyor differ (a) from a standard op-amp and (b) from a current feedback op-amp? Which common device behaves (approximately) like a current conveyor?

[5]

b. Using current conveyors draw circuit diagrams for the following functional blocks:

   i. Voltage amplifier of gain +10
   ii. Gyrator.
   iii. Negative impedance converter
   iv. Full wave precision rectifier
   i. Voltage low pass filter

[10]

c. Design a floating inductor using only grounded capacitors, resistors and current conveyors. Write an expression for the value of the inductor as a function of the components you use.

[5]

4.

a. Figure 4.1 illustrates the type A translinear gain cell. The currents $(1 \pm Y)I_Y$ and $(1 \pm X)I_X$ correspond to the output and the input currents respectively. I_X and I_Y are dc currents whereas Y and X are the output and the input modulation indices respectively.

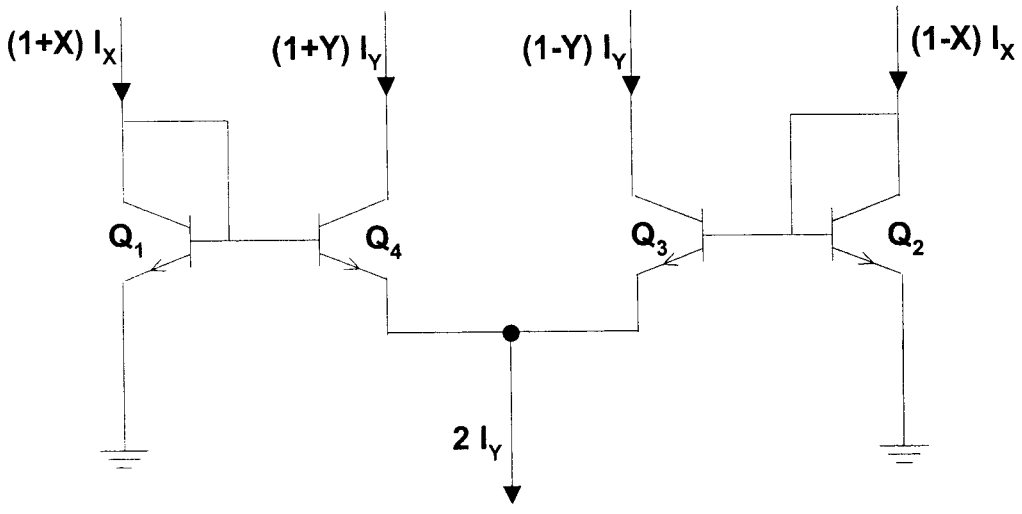


Figure 4.1

i. Show that $X = Y$ and calculate the differential current gain. **[2]**

ii. Assuming that all the transistors are matched show that the circuit operation is immune to the value of β (beta). **[2]**

b. For the circuit of Figure 4.2, I_1 and I_3 are the input currents whereas I_2 and I_4 are constant bias currents. Derive an expression for the output current I_{out} stating any assumptions that you make, and hence outline the function of this circuit. Write down an expression for the output current when $I_1 = \left| \int I_{in}\, dt \right|$ and $I_3 = \left| \frac{dI_{in}}{dt} \right|$, given that $I_{in} = A\sin(\omega t)$. **[8]**

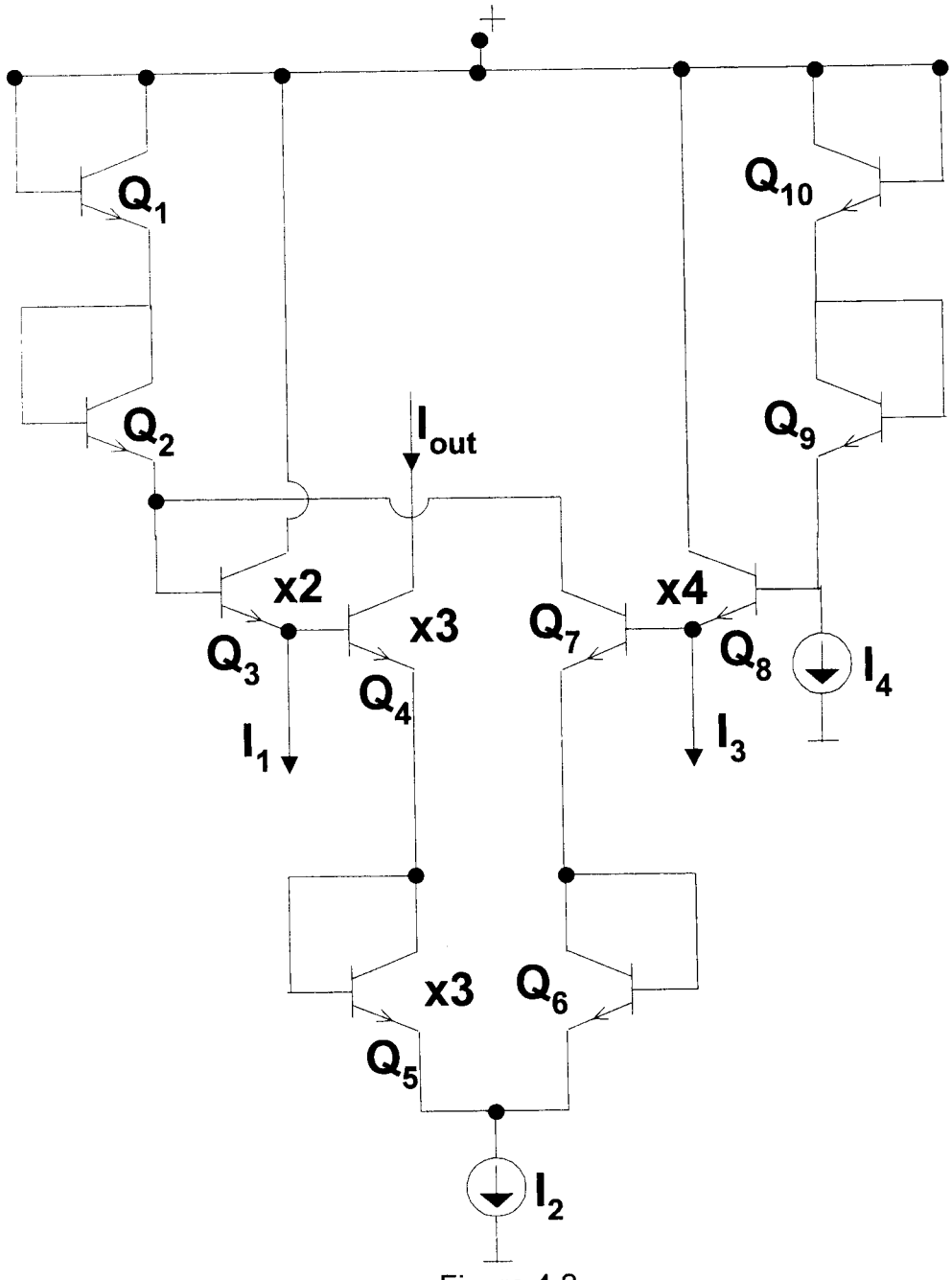


Figure 4.2

c. For the circuit of Figure 4.3, I_{X_1} and I_{X_2} are input currents whereas I_Z is the output current. Express the current I_Z as a function of the currents I_{X_1} and I_{X_2} and the emitter area A. When $I_{X_1} = I_{X_2} = I$, determine the value of the emitter area A for which $I_Z = I$. **[8]**

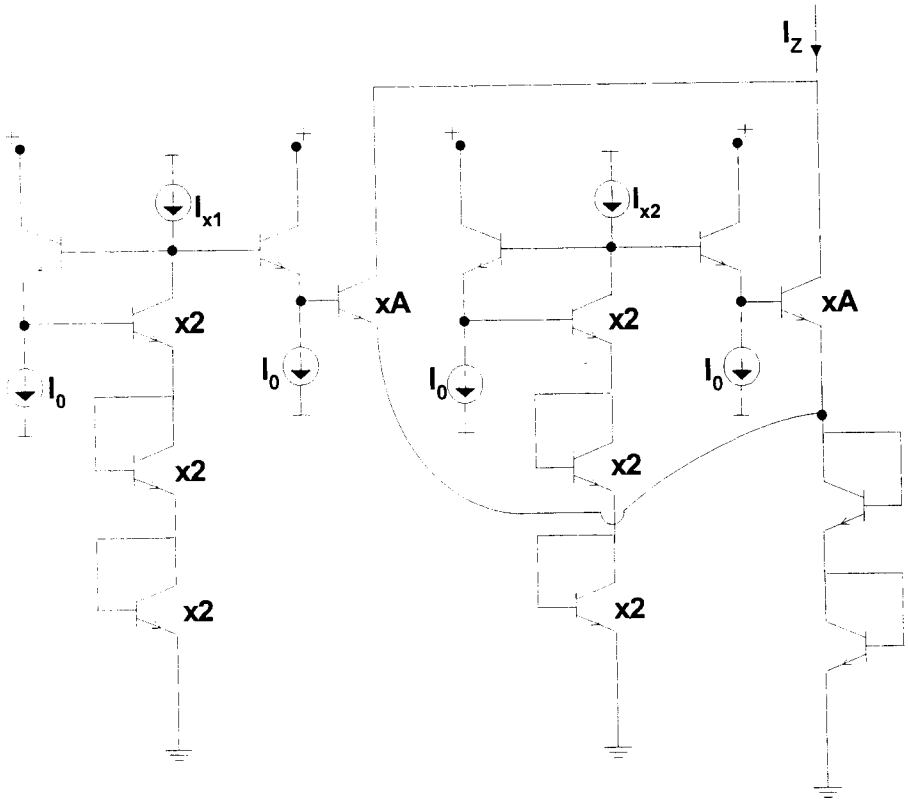


Figure 4.3

5.

a. Figure 5.1 illustrates a general companding circuit.

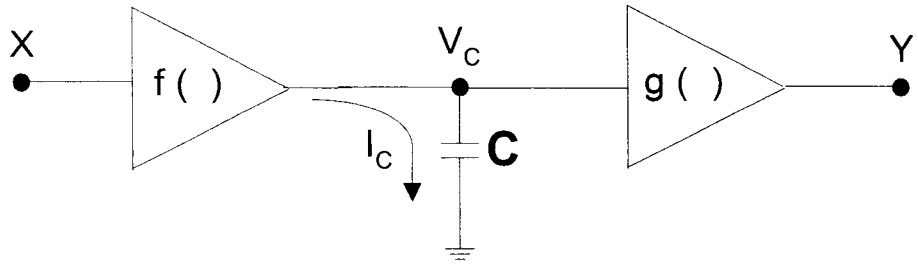


Figure 5.1

i. Derive the condition under which the circuit operates as an input-output linear integrator. **[2]**

ii. If the input signal X is a current of value I_{in} and the output signal Y is a current $I_S exp\left(\frac{V_C}{V_T}\right) = g(V_C)$ determine the function $f(X) = f(I_{in})$ needed for the circuit to operate as an input-output linear companding integrator. **[2]**

b. The transfer function for a second order topology has been decomposed into the following state-space equations:

$$\dot{x}_1 = -\left(\frac{\omega_0}{Q}\right)x_1 - \omega_0 x_2 + \omega_0 U_1$$
$$\dot{x}_2 = \omega_0 x_1 - \omega_0 U_2$$
$$y = x_1$$

where y is the output, x_1 and x_2 are state-variables and U_1 and U_2 are inputs (a dot above a variable denotes time-differentiation).

i. Show that when the input $U_2 = 0$ then the output can be used to implement a second order bandpass transfer function. **[1]**

ii. Show that when the input $U_1 = 0$ then the output can be used to implement a second order lowpass transfer function. **[1]**

iii. Using the exponential mappings $x_j = I_0 exp\left(\frac{V_j}{V_T}\right)(j = 1,2)$,

$U_2 = I_0 exp\left(\frac{V_{U_2}}{V_T}\right)$ and $U_1 = I_S exp\left(\frac{V_{U_1}}{V_T}\right)$ show that the above linear state-space equations can be transformed into non-linear log-domain design equations.

(I_S denotes the reverse saturation current of a bipolar junction transistor) **[6]**

iv. Sketch a transistor-level implementation of a log-domain topology which realises these design equations. **[8]**

6.

a. The following state-space describes the dynamics of a lossy integrator:

$$\dot{x}_1 = -\omega_0 x_1 + \omega_0 U$$
$$y = x_1$$

where y is the output, x is the state-variable and U is the input (a dot above a variable denotes time-differentiation)

i. Using the exponential mappings $x_1 = I_1 exp\left(\frac{V_1}{V_T}\right)$ and

$U = I_U exp\left(\frac{V_U}{V_T}\right)$ show

that the above linear state-space equations can be transformed into non-linear log-domain design equations. **[1]**

ii. From these design equations sketch a transistor-level implementation of a log-domain topology when

$I_1 = I_0$ and $I_U = I_S$, and when **[3]**

$I_1 = I_U = I_0$. **[3]**

(I_S denotes the reverse saturation current of a bipolar junction transistor)

b. State the relation which must be satisfied by two N-port networks, if these two networks are to be considered adjoint networks. Exploiting this relation derive the adjoint network of a resistor, a nullor and an open-loop "ideal" voltage amplifier **[4]**

c. Figure 6.1 illustrates a voltage-mode Sallen-Key biquad implemented by means of voltage amplifiers. Derive its current-mode equivalent. **[2]**

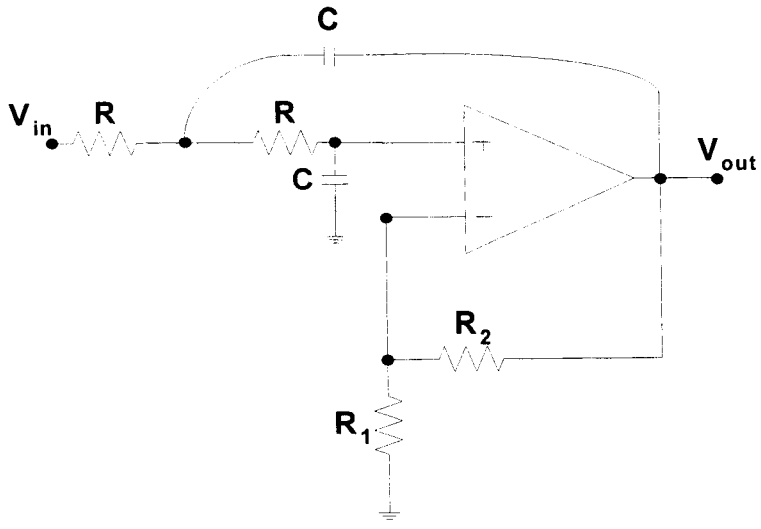


Figure 6.1

d. You are asked to implement a V-I converter. What kind of amplifier would you choose to use if :

i. high-gain ideal amplifiers of any of the four kinds were available to you. **[1]**

ii. only practical amplifiers were available to you. **[1]**

iii. if high-performance current-followers and voltage-followers were available to you. **[1]**

e. Figure 6.2 illustrates a practical current-conveyor.

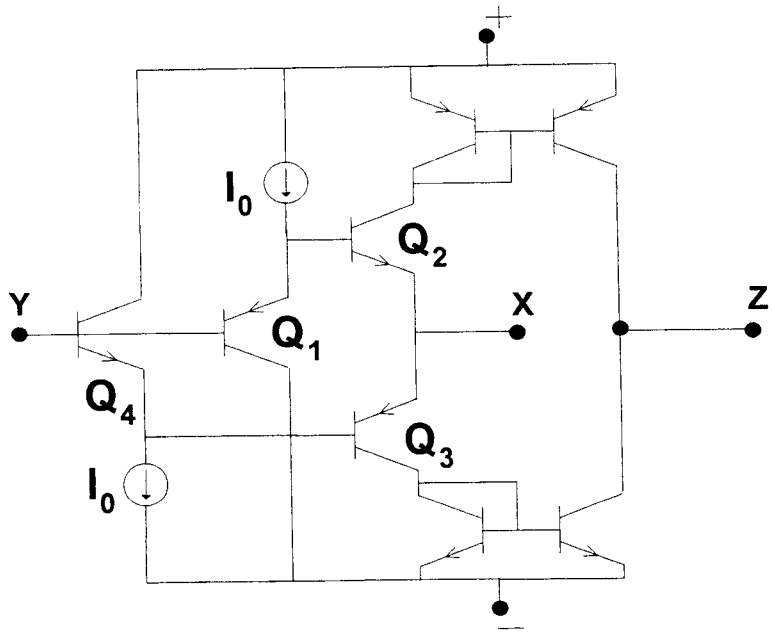


Figure 6.2

i. Draw an elementary current-conveyor and compare its properties with those of Figure 6.2 . **[2]**

ii. Suggest and draw a new current-conveyor of reduced offset. What are the new topology trade-offs with respect to the current-conveyor of Figure 6.2 ? **[2]**

E 4.16/A05

Current-Mode Analogue Signal Processing

1.

(a) Design a unit delay switched current cell of current gain N, both for positive and negative N. What is the maximum signal frequency on which this cell can operate?

[5]

(b) Design a switched current Infinite Impulse Response filter implementing the following transfer function:

$\frac{i_o}{i_i} = \frac{z-1}{z+1}$, at a sampling rate of 1kHz. Specify the clock frequency.

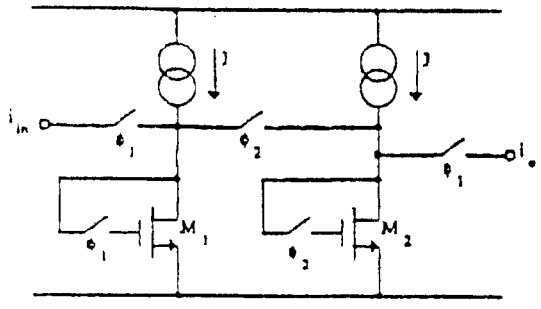
[10]

(c) Discuss 3 limitations of switched current cells, and propose solutions that alleviate these limitations. Draw relevant diagrams.

[4]

Answer 1.a Bookwork+ interpretation

A SI cell implements half a unit delay, i.e. half a period delay at the clock rate:
$i_o / i_i = -z^{-1/2}$.
If the gain of the delay element is negative it can be implemented with one cell, and half the switching frequency. If the gain of the delay element is positive two cells need to be cascaded for a unit delay.



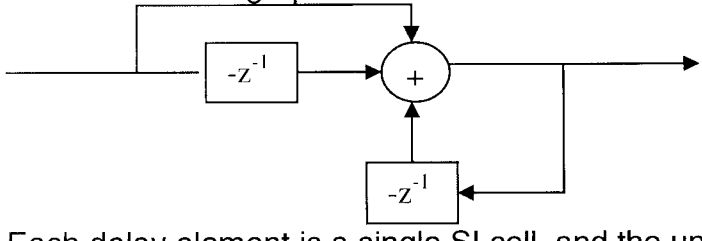
The sampling theorem applies in a SI circuit, so maximum signal frequency is $f_{clock}/2$, in both cases. In practice signals are restricted to $f_{clock}/10$. The current gain is M_1 for the inverting delay, and $M_1 M_2$ for the non inverting.

[5]

Answer 1.b Computed example

$$\frac{i_o}{i_i} = \frac{z-1}{z+1} \Rightarrow i_o(z+1) = i_i(z-1) \Rightarrow i_o = -z^{-1} i_o + i_i - z^{-1} i_i$$

this has the flow graph:

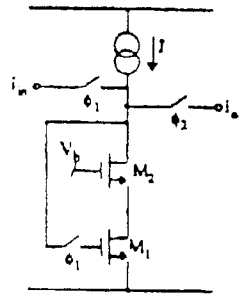


Each delay element is a single SI cell, and the unit undelayed path can be a current mirror

[10]

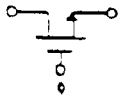
Answer 1.c Bookwork

- Finite drain conductance leads to gain error. Cascoded cell alleviates this:

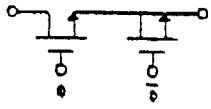


- Charge injection to the gate. Gain error and harmonic distortion. Dummy switches alleviate this:

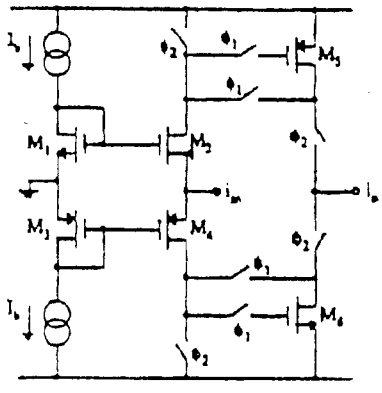
Simple switch



Dummy switch compensation



- Signal swing: Can be improved by duplicating the circuit in the opposite gender (class AB):



2.

(a) Draw a diagram for the standard 3 op-amp instrumentation amplifier, and describe its operation and advantages over a single op-amp difference amplifier.

[4]

(b) Draw a diagram for a current mode instrumentation amplifier. What advantages does it have over the voltage mode instrumentation amplifier?

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(c) Describe the current feedback op-amp, and draw a transistor level diagram of a commercial current feedback op-amp. Explain why a current feedback op-amp has a theoretically infinite slew rate.

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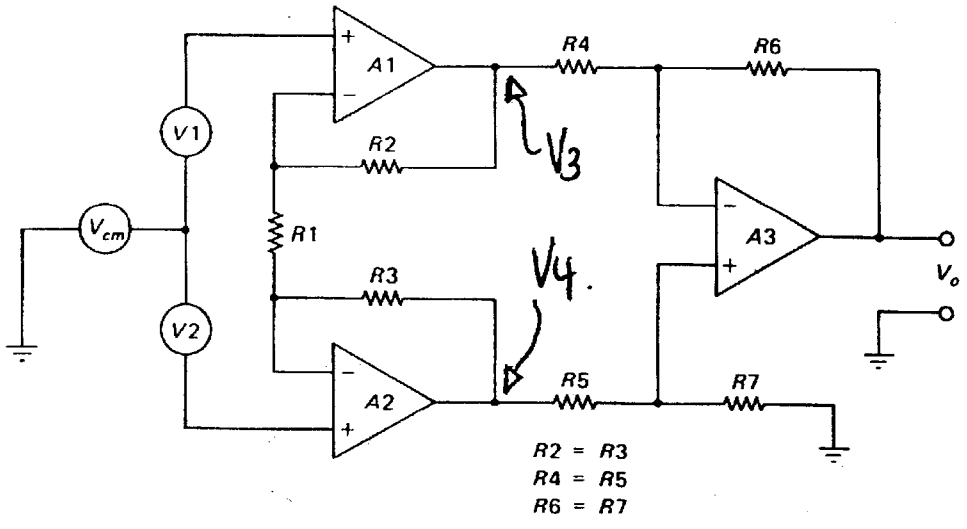
(d) Draw circuit diagrams to show how if, and how, a current feedback op-amp can be used to implement:

i. An inverting voltage amplifier of gain 10
ii. A non inverting voltage amplifier of gain 6
iii. A low pass filter with a pole at zero frequency.

[6]

Answer 2.a Bookwork

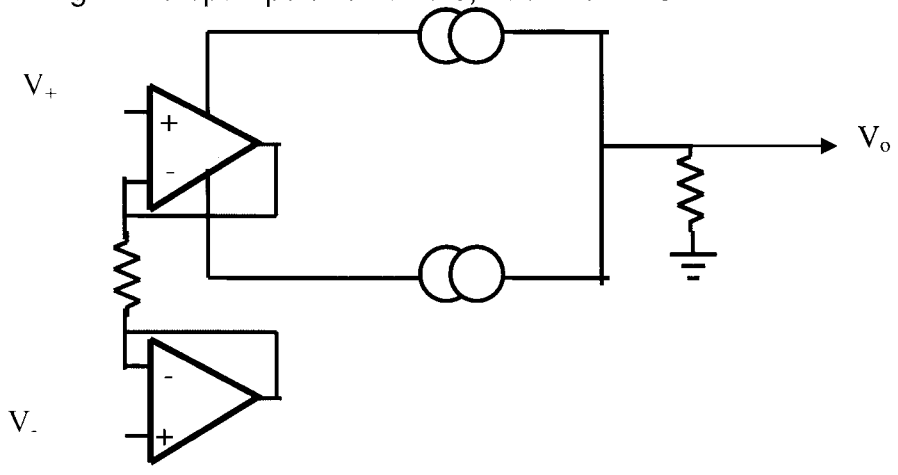
3 op-amp instrumentation amplifier:
1st stage has differential gain >1, and common mode gain approx. 1. This configuration has high CMRR, subject to the close matching of resistors, e.g as indicated.



[4]

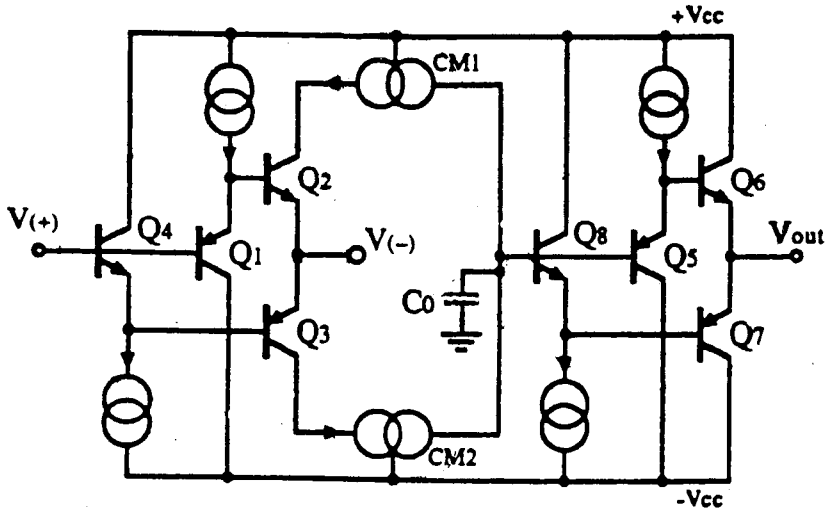
Answer 2.b Bookwork

Can obviate the need for most resistors by using the supply sensing technique. This is still a difference amplifier, with differential gain equal to the ratio of the resistors. Needs good matching of the opamps and mirrors, has inferior CMRR.



[4]

A commercial CFOA:



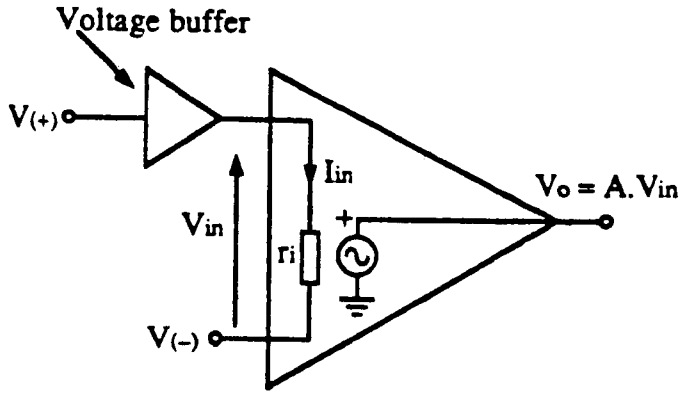
The input voltage folleower has a transconductance function:

$g_m \propto \sinh(v_{in})$ and hence an infinite theoretical slew rate, since $\lim i_{v\to\infty} = \infty, \frac{dV}{dt} \propto \frac{i}{C_o}$

[6]

Answer 2.c Bookwork

A CFOA is a differential transimpedance amplifier with a unity voltage buffer at the non-inverting input.



Answer 2.d Computed example

The inverting and non-inverting amplifiers are designed exactly as with voltage feedback op-amps (resistor ratios 10 and 5 respectively) . The ideal integrator is impossible because a pure capacitive feedback will render the circuit unstable.

[6]

3.

(a) Describe the current conveyor. How does a second generation current conveyor differ from a first generation current conveyor? How does a current conveyor differ from a standard op-amp? From a current feedback op-amp? Which common device behaves (approximately) like a current conveyor?

[5]

(b) Using current conveyors draw circuit diagrams for the following functional blocks:

i. Voltage amplifier of gain +10
ii. Gyrator.
iii. Negative impedance converter
iv. Full wave precision rectifier
i. Voltage low pass filter

[10]

(c) Design a floating inductor using only grounded capacitors, resistors and current conveyors. Write an expression for the value of the inductor as a function of the components you use.

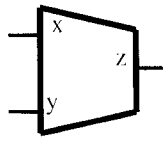
[5]

Answer 3.a Bookwork

A current conveyor has the transfer function

$$\begin{bmatrix} V_x \\ i_y \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_x \\ V_y \\ V_z \end{bmatrix}$$ the first generation conveyor has a finite current into the voltage (y) terminal. The current conveyor and opamp comparison:

	+in	-in	Out
CC	V	I	I
OA	V	V	V
CFOA	V	I	V

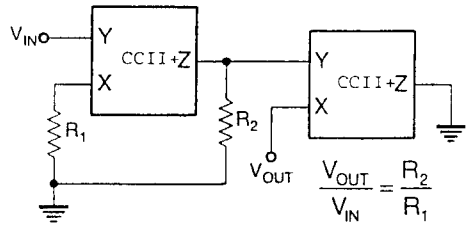


A BJT approximates a Current Conveyor.

[5]

Answer 3.b Bookwork

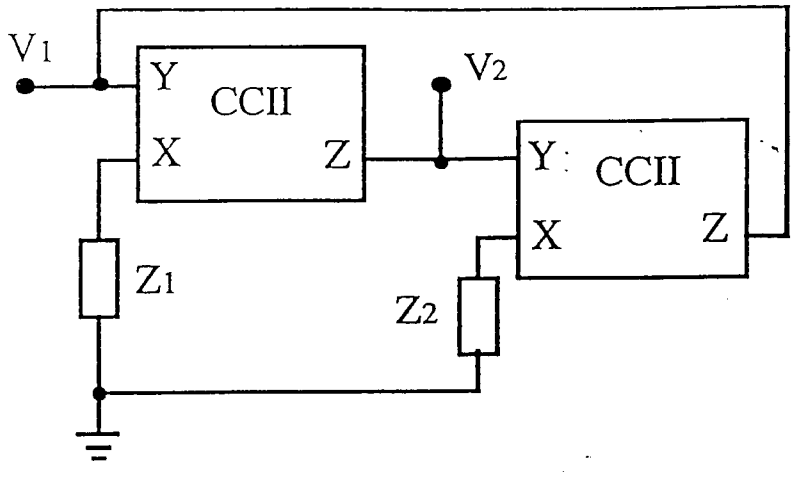
i. Voltage amplifier of gain +10



$$\frac{R_2}{R_1} = 10$$

[2]

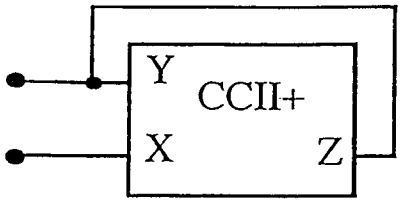
ii. Gyrator.



$$Z_{in} = \frac{R_1 R_2}{Z_2}$$

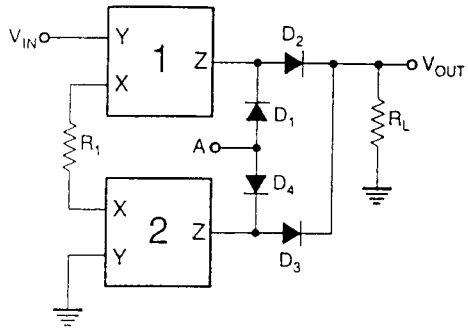
[2]

iii. Negative impedance converter



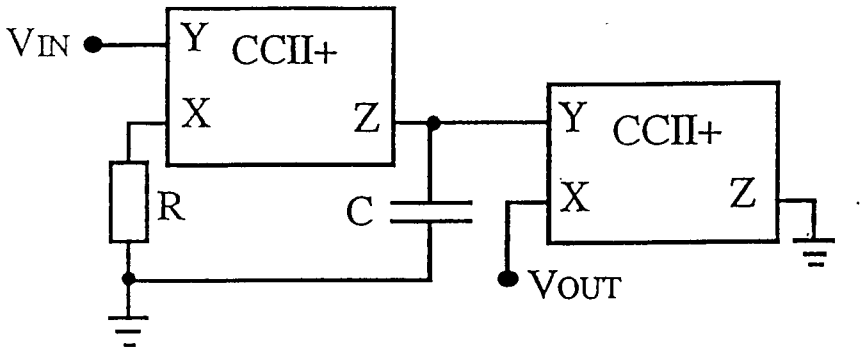
[2]

iv. Full wave precision rectifier



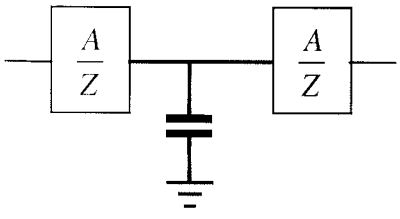
[2]

v. Voltage low pass filter



[2]

Answer 3.c Computed example



where $A = R_1 R_2$ using the gyrator in 3biii. Then $L = \frac{A}{C}$

[5]

Question 4

10/22 22

(a) i) Applying TLP & neglecting beta-errors:

$$(1+x)I_x(1-y)I_y = (1+y)I_y(1-x)I_x \Rightarrow$$

$$\Rightarrow \quad y = x$$

Differential gain:

$$\left.\begin{aligned}\frac{(1+y)I_y-(1-y)I_y}{(1+x)I_x-(1-x)I_x} &= \frac{2yI_y}{2xI_x}\end{aligned}\right\} \Rightarrow$$

But $y = x$

$$\Rightarrow \boxed{\text{Differential gain} = \frac{I_y}{I_x}} \quad (2)$$

ii) Assuming that all transistors are matched & letting $\delta = \frac{1}{\beta}$ or $\frac{1}{\beta+1}$ $\Rightarrow$

$$\left.\begin{aligned}&\text{base current of } Q_1 \simeq \delta(1+x)I_x\\ &\text{-"- -"- -"- } Q_4 \simeq \delta(1+y)I_y\\ &\text{-"- -"- -"- } Q_3 \simeq \delta(1-y)I_y\\ &\text{-"- -"- -"- } Q_2 \simeq \delta(1-x)I_x\end{aligned}\right\} \Rightarrow$$

$$\left.\begin{aligned}I_{C_1} &= (1+x)I_x(1-\delta) - \underbrace{\delta(1+y)I_y}_{I_{B4}}\\ I_{C_2} &= (1-x)I_x(1-\delta) - \underbrace{\delta(1-y)I_y}_{I_{B3}}\end{aligned}\right\} \Rightarrow \text{Applying TLP} \Rightarrow$$

$$\Rightarrow \quad I_{C_1}I_{C_3} = I_{C_2}I_{C_4} \Rightarrow \Big[\underbrace{(1+x)I_x(1-\delta)-\delta(1+y)I_y}_{I_{C_1}}\Big](1-y)I_y =$$

$$= \Big[\underbrace{(1-x)I_x(1-\delta)-\delta(1-y)I_y}_{I_{C_2}}\Big](1+y)I_y$$

The relation is satisfied for $Y = X$ despite the inclusion of the beta errors $1/\beta$! (9)

(b) Applying TLP along $Q_1 Q_2 Q_3 \ldots Q_8 Q_9 Q_{10}$ $\Rightarrow$ & neglecting any beta errors

$\Rightarrow$ I_{C_1} I_{C_2} $\frac{I_{C_3}}{2}$ $\frac{I_{C_4}}{3}$ $\frac{I_{C_5}}{3}$ $= I_{C_6}$ I_{C_7} $\frac{I_{C_8}}{4}$ I_{C_9} $I_{C_{10}}$ $\Rightarrow$

(I_1, I_{out}, I_{out}, I_3; $I_{C_1} = I$, $I_{C_2} = I$, $I_{C_6} = I$, $I_{C_7} = I$, $I_{C_9} = I_4$, $I_{C_{10}} = I_4$)

$\Rightarrow$ $I^2 \frac{I_1}{2} \left(\frac{I_{out}}{3}\right)^2 = I^2 \frac{I_3}{4} I_4^2 \Rightarrow$

$\Rightarrow$ $\left(\frac{I_{out}}{3}\right)^2 = \frac{\left(\frac{I_3}{4}\right)}{\left(\frac{I_1}{2}\right)} I_4^2 \Rightarrow$

$\Rightarrow$ $\left(\frac{I_{out}}{3}\right)^2 = \frac{1}{2}\left(\frac{I_3}{I_1}\right) I_4^2 \Rightarrow$

$$\boxed{I_{out} = \left(\frac{3}{\sqrt{2}}\right)\sqrt{\frac{I_3}{I_1}}\, I_4}$$

$I_{in} = A\sin(\omega t) \Rightarrow \frac{dI_{in}}{dt} = (A\omega)\cos(\omega t)$

$\frac{d\cos(\omega t)}{dt} = -\omega \sin(\omega t) \Rightarrow -\frac{\cos(\omega t)}{\omega} = \int \sin(\omega t)\, dt \Rightarrow$

$\Rightarrow$ When $I_{in} = A\sin(\omega t) \Rightarrow \int I_{in}\, dt = \int A\sin(\omega t)\, dt = -\frac{A}{\omega}\cos(\omega t)$ $\Rightarrow$

$$\left.\begin{aligned} \left|\int I_{in}\,dt\right| &= \frac{A}{w}\,|\cos(wt)| = I_1 \\ \left|\frac{dI_{in}}{dt}\right| &= Aw\,|\cos(wt)| = I_3 \end{aligned}\right\} \Rightarrow$$

$$\frac{I_3}{I_1} = \frac{Aw\,|\cos(wt)|}{\frac{A}{w}\,|\cos(wt)|} = w^2 \Rightarrow$$

$$I_{out} = \frac{3}{\sqrt{2}}\,w\,I_4 \quad \text{when} \quad \frac{I_3}{I_1} = w^2 \Rightarrow$$

$$\Rightarrow I_{out} = \left(\frac{3}{\sqrt{2}}I_4\right)w = Kw \Rightarrow$$

($\frac{3}{\sqrt{2}}I_4$: constant)

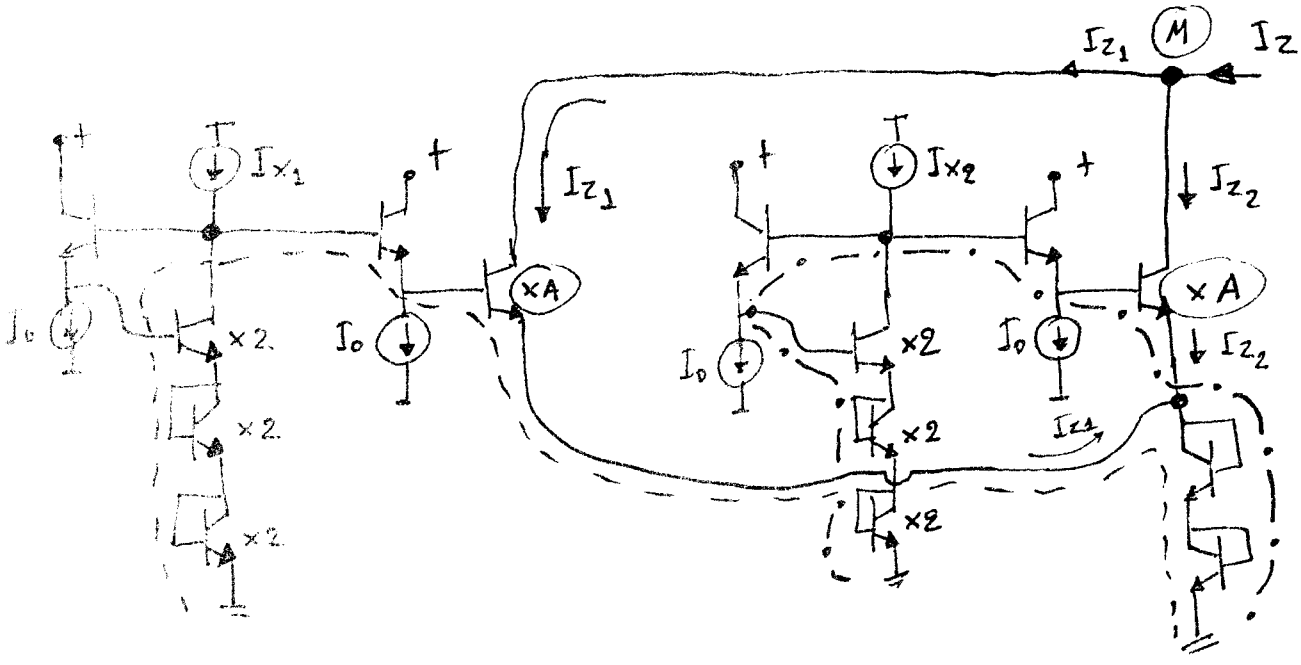
$\Rightarrow$ The circuit operates as a frequency-to-I converter!

(8)

(c)

Applying TLP :

$$\left.\begin{aligned} \frac{I_{x_1}}{2}\ \frac{I_{x_1}}{2}\ \frac{I_{x_1}}{2}\ I_o &= I_o\ \frac{I_{z_1}}{A}\ (I_{z_1}+I_{z_2})^2 \\ \frac{I_{x_2}}{2}\ \frac{I_{x_2}}{2}\ \frac{I_{x_2}}{2}\ I_o &= I_o\ \frac{I_{z_2}}{A}\ (I_{z_1}+I_{z_2})^2 \end{aligned}\right\} \Rightarrow$$



$$\Rightarrow \left[\left(\frac{I_{x_1}}{2}\right)^3 + \left(\frac{I_{x_2}}{2}\right)^3\right] I_o = I_o\ (I_{z_1}+I_{z_2})^2\ \frac{I_{z_1}+I_{z_2}}{A} \Bigg\} \Rightarrow$$

But from KCL at (M) $\Rightarrow I_{z_1}+I_{z_2}=I_z$

$$\Rightarrow \frac{I_z^3}{A} = \frac{I_{x_1}^3+I_{x_2}^3}{2^3} \Rightarrow \boxed{I_z = \frac{A^{1/3}}{2}\ \sqrt[3]{I_{x_1}^3+I_{x_2}^3}}$$

When $I_{x_1} = I_{x_2} = I \Rightarrow$

$$\Rightarrow I_z = \frac{A^{1/3} Z^{1/3}}{2} I$$

$$I_z = I \Rightarrow \frac{A^{1/3} Z^{1/3}}{2} = 1 \Rightarrow$$

$$\Rightarrow A^{1/3} = Z^{2/3} \Rightarrow$$

$$\Rightarrow \boxed{A = 4} !$$

(8)

Question 5

(a) i) $Y = g(V_c)$

$$I_c = f(x) = C\frac{dV_c}{dt}$$

I require $\frac{dY}{dt} = KX \iff Y = K\int X\,dt \Rightarrow$ input-output linear integration)

But $\frac{dY}{dt} = \frac{dg(V_c)}{dV_c}\frac{dV_c}{dt} = \frac{dg(V_c)}{dV_c}\frac{I_c}{C} = \frac{dg(V_c)}{dV_c}\frac{f(x)}{C} \Rightarrow$

$$\Rightarrow \boxed{\frac{dg(V_c)}{dV_c}\frac{f(x)}{C} = X}$$ ← condition for linear integration (2)

ii) $Y = I_{out} = I_S \exp\left(\frac{V_c}{V_T}\right) = g(V_c)$

$$\frac{dY}{dV_c} = \frac{dg(V_c)}{dV_c} = \frac{I_S \exp(V_c/V_T)}{V_T} = \frac{I_{out}}{V_T}$$

From the general condition for input-output linear integration we require

$$\frac{dY}{dV_c}\frac{f(x)}{C} = KX \Rightarrow$$

$$f(x) = \frac{KC}{\left(\frac{dY}{dV_c}\right)}X = \frac{KCV_T}{I_{out}}X = X\frac{I_0}{I_{out}} \Rightarrow$$

$$f(I_{in}) = \frac{I_{in}I_0}{I_{out}} = \text{translinear relation}$$ (2)

(b)

$$\dot{x}_1 + \left(\frac{\omega_0}{Q}\right) x_1 + \omega_0 x_2 = \omega_0 v_1$$

$$-\omega_0 x_1 + \dot{x}_2 = -\omega_0 v_2$$

$$y = x_1$$

i) $v_2 = 0 \Rightarrow$

$$\left(s + \frac{\omega_0}{Q}\right) X_1(s) + \omega_0 X_2(s) = \omega_0 V_1(s)$$

$$-\omega_0 X_1(s) + s X_2(s) = 0$$

$$Y(s) = X_1(s)$$

$$\Rightarrow X_1(s) = \frac{\begin{vmatrix} \omega_0 V_1(s) & \omega_0 \\ 0 & s \end{vmatrix}}{\begin{vmatrix} s + \frac{\omega_0}{Q} & \omega_0 \\ -\omega_0 & s \end{vmatrix}} = \frac{\omega_0 s V_1(s)}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \Rightarrow$$

Bandpass TF

$$\frac{X_1(s)}{V_1(s)} = \frac{Y(s)}{V_1(s)} = \frac{\omega_0 s V_1(s)}{s^2 + \left(\frac{\omega_0}{Q}\right) s + \omega_0^2}$$ (1)

ii) $v_1 = 0 \Rightarrow$

$$\left(s + \frac{\omega_0}{Q}\right) X_1(s) + \omega_0 X_2(s) = 0$$

$$-\omega_0 X_1(s) + s X_2(s) = -\omega_0 V_2(s)$$

$$Y(s) = X_1(s)$$

$$X_1(s) = \frac{\begin{vmatrix} 0 & \omega_0 \\ -\omega_0 V_2(s) & s \end{vmatrix}}{s^2 + \left(\frac{\omega_0}{Q}\right) s + \omega_0^2} = \frac{\omega_0^2 V_2(s)}{s^2 + \left(\frac{\omega_0}{Q}\right) s + \omega_0^2} \Rightarrow$$

$$\frac{Y(s)}{V_2(s)} = \frac{\omega_0^2}{s^2 + \left(\frac{\omega_0}{Q}\right) s + \omega_0^2}$$ ← Lowpass TF (1)

iii)

$$x_1 = I_o\, e^{\frac{V_1}{V_T}} \Rightarrow \dot{x}_1 = \frac{\dot{V}_1}{V_T} x_1$$

$$x_2 = I_o\, e^{\frac{V_2}{V_T}} \Rightarrow \dot{x}_2 = \frac{\dot{V}_2}{V_T} x_2$$

$$\left.\begin{aligned} \frac{\dot{V}_1}{V_T} x_1 + \left(\frac{w_o}{Q}\right) x_1 + w_o x_2 &= w_o I_s\, e^{\frac{V_{U_1}}{V_T}} \\ \frac{\dot{V}_2}{V_T} x_2 - w_o x_1 &= -w_o I_o\, e^{\frac{V_{U_2}}{V_T}} \end{aligned}\right\} \Rightarrow$$

$$\Rightarrow \left.\begin{aligned} C\dot{V}_1 + \frac{(CV_T w_o)}{Q} I_o + (CV_T w_o)\, e^{\frac{V_2 - V_1}{V_T}} I_o &= (CV_T I_o) \frac{I_s}{I_o}\, e^{\frac{V_{U_1} - V_1}{V_T}} \\ C\dot{V}_2 - (CV_T w_o)\, e^{\frac{V_1 - V_2}{V_T}} I_o &= -(CV_T w_o) \frac{I_o}{I_o}\, e^{\frac{V_{U_2} - V_2}{V_T}} I_o \end{aligned}\right\} \Rightarrow$$

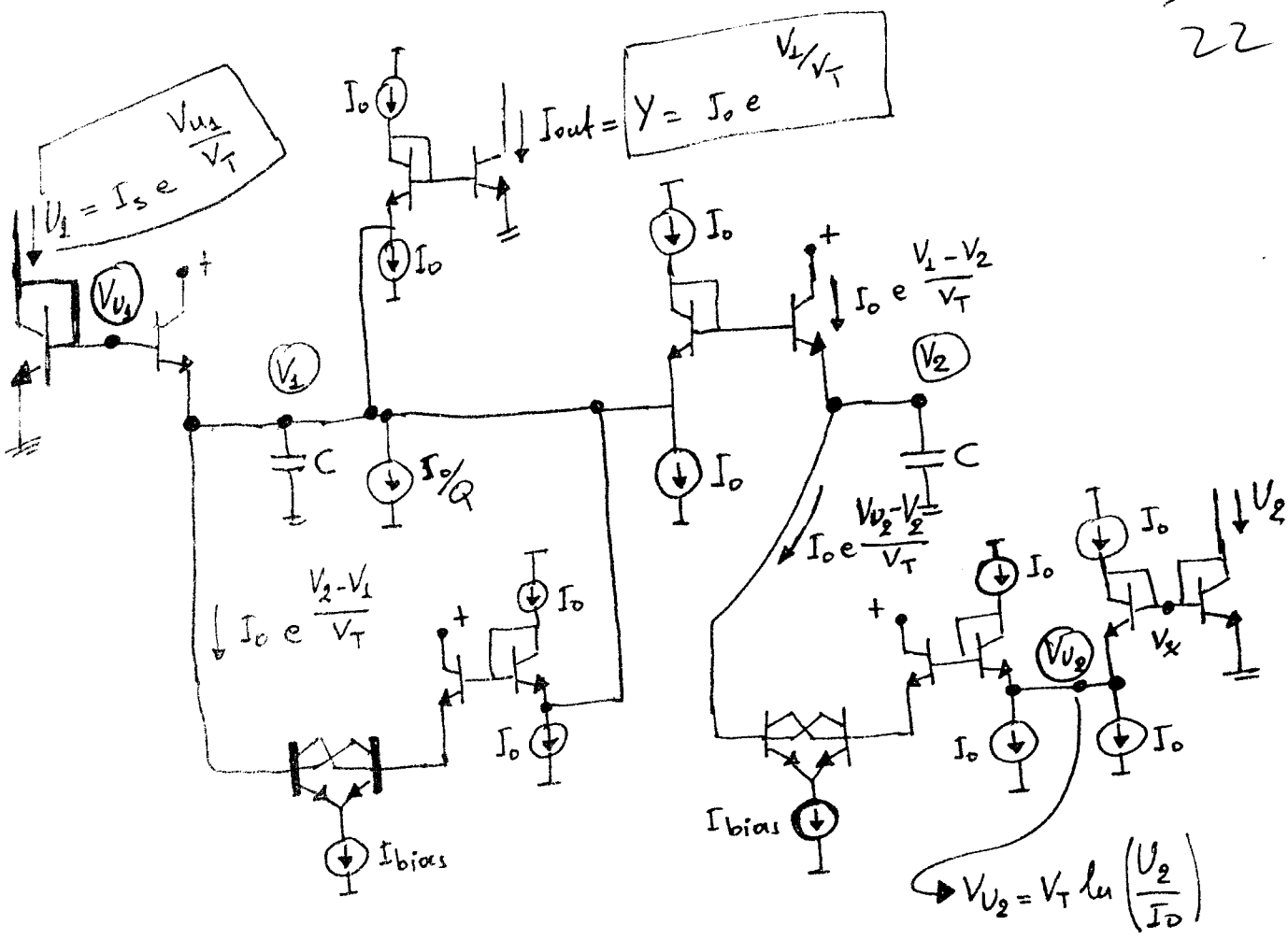
$$\boxed{\begin{aligned} C\dot{V}_1 + \frac{I_o}{Q} + I_o\, e^{\frac{V_2 - V_1}{V_T}} &= I_s\, e^{\frac{V_{U_1} - V_1}{V_T}} \\ C\dot{V}_2 + I_o\, e^{\frac{V_{U_2} - V_2}{V_T}} &= I_o\, e^{\frac{V_1 - V_2}{V_T}} \end{aligned}}$$

Log-domain (Non-linear) Design equations

$$\boxed{Y = I_o\, e^{V_1/V_T}}$$

(6)

(iv)



$$V_x = V_T \ln\left(\frac{V_2}{I_S}\right)$$

$$V_x - V_T \ln\left(\frac{I_0}{I_S}\right) = V_T \ln\left(\frac{V_2}{I_D}\right) = V_{U_2} \Rightarrow$$

$$\boxed{V_2 = I_0 e^{\frac{V_{U_2}}{V_T}}}$$

8

Question 6

(a) (i) $\dot{x}_1 + \omega_0 x_1 = \omega_0 U$, $y = x_1$ $\Big\}$ $x_1 = I_1 e^{V_1/V_T} \Rightarrow \dot{x}_1 = x_1 \frac{\dot{V}_1}{V_T}$ $\Big\}$ $\Rightarrow$

$\Rightarrow$ $\Rightarrow$ $U = I_U e^{V_U/V_T}$

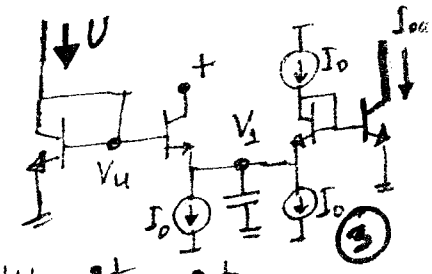
$\Rightarrow$ $x_1 \frac{\dot{V}_1}{V_T} + \omega_0 x_1 = \omega_0 I_U e^{V_U/V_T}$, $y = I_1 e^{V_1/V_T}$ $\Big\}$ $\Rightarrow$

$\Rightarrow$ $C\dot{V}_1 + (CV_T\omega_0) = (CV_T\omega_0)\frac{I_U}{I_1} e^{\frac{V_U - V_1}{V_T}}$, $x = I_1 e^{V_1/V_T}$ $\Big\}$ $\Rightarrow$

$\Rightarrow$ (I set $CV_T\omega_0 = I_0$) $\Rightarrow$

$\Rightarrow$ $C\dot{V}_1 + I_0 = \frac{I_0 I_U}{I_1} e^{\frac{V_U - V_1}{V_T}}$, $y = I_1 e^{V_1/V_T}$ ... (1)

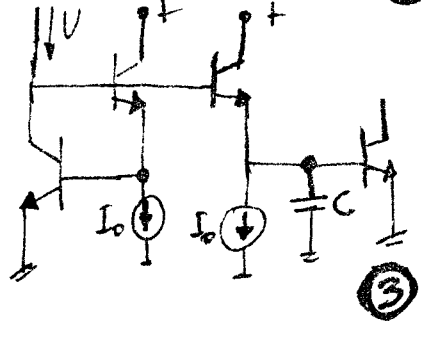
(b) $I_1 = I_0$ & $I_U = I_S$ $\Rightarrow$ $C\dot{V}_1 + I_0 = I_S e^{\frac{V_U - V_1}{V_T}}$, $x = I_0 e^{V_1/V_T}$ $\Rightarrow$



(3)

(c) $I_1 = I_U = I_0$ $\Rightarrow$ $C\dot{V}_1 + I_0 = I_0 e^{\frac{V_U - V_1}{V_T}}$ $\Rightarrow$

$y = I_0 e^{V_1/V_T}$



(3)

(b) Two N-port networks A & B are adjoint when

$$\sum_{n=1}^{N} \left(V_{An} I_{Bn} - V_{Bn} I_{An}\right) = 0$$

with V_{An} denoting the voltage of the n-th port of network A, etc...

- **Resistor**, $V_A = R_A I_A$, one port

$$V_A I_B - V_B I_A = 0 \Rightarrow \frac{V_B}{I_B} = \frac{V_A}{I_A} \Rightarrow$$

But $\frac{V_A}{I_A} = R_A$

$\Rightarrow V_B = I_B \cdot \underbrace{R_A}_{R_B}$, Hence the adjoint of a resistor is a resistor of the same value

- **Nullor**

$V_A = [V_{A1}\ V_{A2}] = [0\ X]$

$I_A = [I_{A1}\ I_{A2}] = [0\ X]$

X denotes "any value"

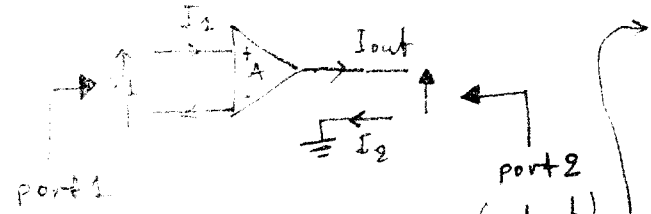
Hence I want: $V_{A1} I_{B1} - V_{B1} I_{A1} + V_{A2} I_{B2} - V_{B2} I_{A2} = 0$ ($V_{A1}: 0$, $I_{A1}: 0$, $V_{A2}: X$, $I_{A2}: X$)

Hence when $V_B = [V_{B1}\ V_{B2}] = [X\ 0]$

and $I_B = [I_{B1}\ I_{B2}] = [X\ 0]$ the relation is satisfied

Thus the adjoint of a nullor is another nullor with its input & output ports interchanged.

- **Voltage Amplifier**



$V_A = [V_{A1}\ V_{A2}] = [V_{in}\ AV_{in}]$

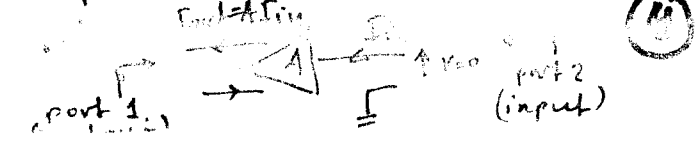
$I_A = [I_{A1}\ I_{A2}] = [0\ X]$

Hence $V_{A1} I_{B1} - V_{B1} I_{A1} + V_{A2} I_{B2} - V_{B2} I_{A2} = 0$ ($V_{A1}: V_{in}$, $I_{A1}: 0$, $V_{A2}: AV_{in}$, $I_{A2}: X$)

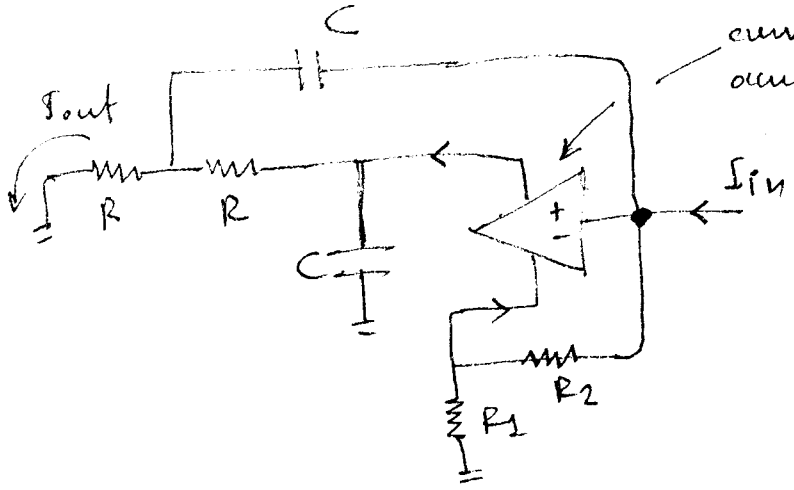
and when $V_B = [V_{B1}\ V_{B2}] = [X\ 0]$

$I_B = [I_{B1}\ I_{B2}] = [-AI_{in}\ I_{in}]$

then the relation is satisfied. Thus the adjoint of an ideal voltage amplifier is a current amplifier with input & output ports



(c)



(2)

(d) i) When high-gain "ideal amplifiers" are available, it doesn't matter what kind of amplifier you use (1)

ii) If practical amplifiers are available then for a V-I converter we should use a VCCS because with this choice the closed-loop bandwidth becomes independent of the source & load resistance. The price paid in this case is that the V-I converter bandwidth cannot be set independently of its gain (gain-bandwidth conflict) (1)

iii) When high-performance CFs & VFs are available then we should choose any other amplifier except from a transconductance amplifier. For if we choose

a buffered transresistance amplifier (CCVS)

or " current " (CCCS)

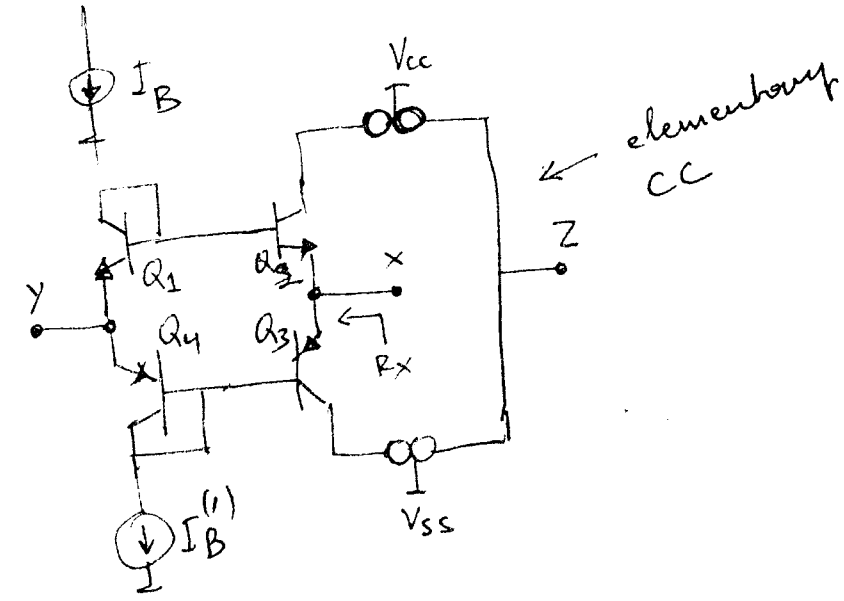
or " voltage " (VCVS) (1)

then the closed loop bandwidth of the converter can be set independently from the closed-loop gain.

Question 6/3

(e)

i)

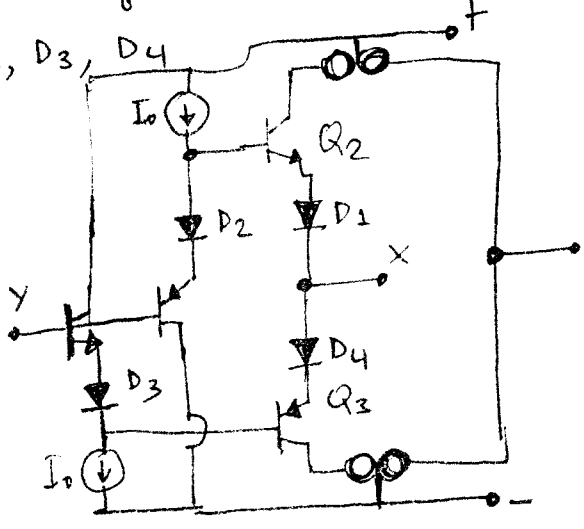


Input offset voltage $\Rightarrow V_X - V_Y = V_{BE_1} - V_{BE_2} \simeq 0$ < input voltage offset for the **practical** CC

$R_X = r_{e_2} \parallel r_{e_3} \simeq R_X$ of the practical CC

Input current offset $\Rightarrow I_y = \Delta I_B = I_B - I_B' >$ input current offset $\frac{\Delta I_B}{\beta}$ for the practical **CC**

ii) Reduced offset voltage can be achieved by including the diodes (diode-connected BJT devices) D_1, D_2, D_3, D_4



D_1 implemented with p-type BJT
D_2 —||— —||— n-type —||—
D_3 —||— —||— p-type —||—
D_4 —||— —||— n-type —||—

$V_y - V_x \simeq 0$ because from Y to X terminal we "meet" two n-type & two p-type base-emitter junctions $\Rightarrow$ matching. However $R_X = (r_{e_2} + r_{D_1}) \parallel (r_{e_3} + r_{D_4}) > r_{e_2} \parallel r_{e_3} = R_X$ for the practical Current Conveyor. The inclusion of D_1, D_2, D_3 & D_4 reduces the input voltage dynamic