Paper Number(s): **E4.16**
**AM3**

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2001

MSc and EEE PART IV: M.Eng. and ACGI

# CURRENT-MODE ANALOGUE SIGNAL PROCESSING

Tuesday, 22 May 10:00 am

There are SIX questions on this paper.

Answer FOUR questions.

Time allowed: 3:00 hours.

Examiners: Toumazou,C. and Burdett,A.J.

**Corrected Copy**

**Special instructions for invigilators**: None

**Information for candidates**: None

1. The circuit shown in *Figure 1* is a typical architecture for a current-feedback op-amp.

a) Very briefly explain the operation of the circuit and comment upon why the slew rate of such an op-amp architecture can potentially be greater than $1000\ V/\mu s$. With the aid of a macro-model, explain the theoretical concept of current-feedback and how it results in constant bandwidth amplification.

***(13 marks)***

b) Explain why the gain-bandwidth product of the amplifier remains almost constant for high values of voltage gain. What is the function of diodes $D_1$ - $D_4$ in the circuit ?

***(8 marks)***

c) Finally, connect the op-amp as a closed-loop non-inverting voltage amplifier and design the amplifier to have a voltage gain of *10* at a fixed bandwidth of approximately *10 MHz*.

***(4 marks)***

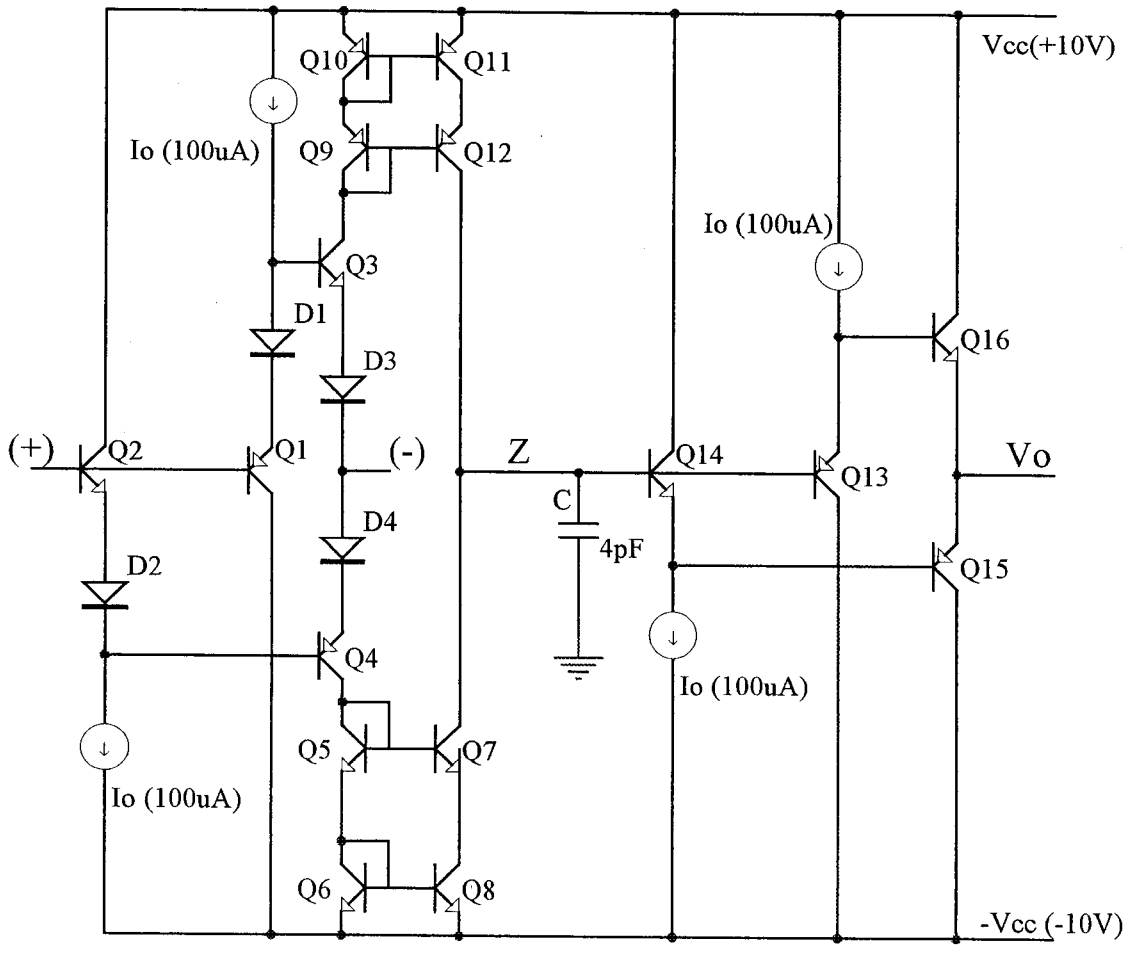



***Figure 1***

2. The circuit of *Figure 2* is a precision switched-current integrator.

a) Derive an expression for the time constant of the integrator. Assume the integrator is driven by non-overlapping clocks and that the switches are ideal.

***(10 marks)***

b) Give two sources of current transmission error in the switched current memory cell, and suggest suitable circuit techniques which will reduce these errors.

***(2 marks)***

c) The current-conveyor is an alternative building block to the operational amplifier for current-mode applications. Sketch a typical circuit for the current-conveyor based upon the use of the power supply leads of the operational amplifier. Connect the current-conveyor as a current-follower and explain why the architecture of amplifier has a very high bandwidth potential.

***(10 marks)***

d) Finally, draw circuits for a current-mode integrator and differentiator using the current-conveyor.

***(3 marks)***

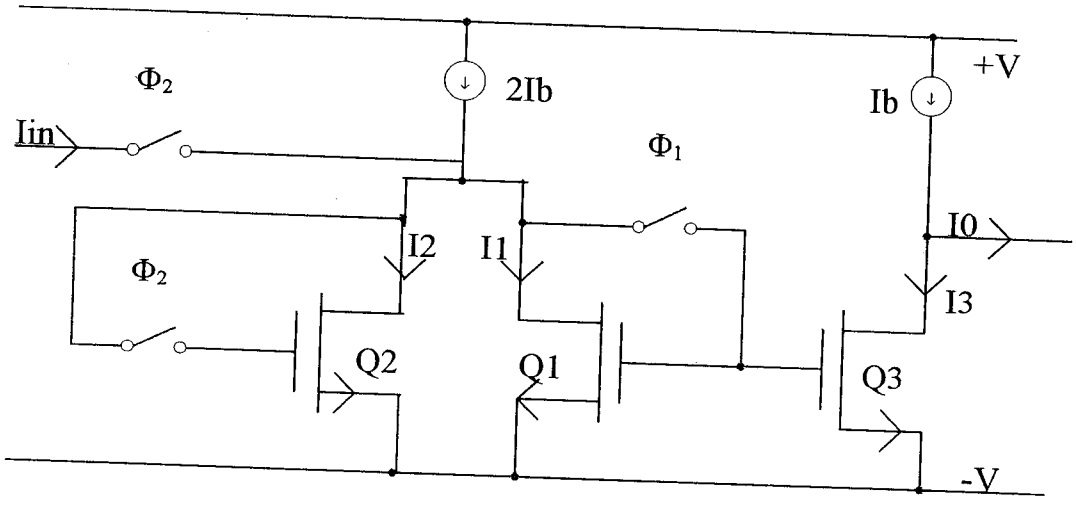



***Figure 2***

3. a) The circuit of *Figure 3(a)* is an instrumentation amplifier. Analyse the circuit to show that the differential voltage gain $AVD = N(2M + 1)$ given that $R1=R3=R7=R$, $R2=R4=NR$ and $R5=R6=MR$. Find the worst case common-mode rejection ratio (CMRR) of the circuit when resistors with $\pm$ 1% tolerance are used.

***(15 marks)***

b) Finally, briefly explain the operation of the circuit in *Figure 3(b)*, and discuss advantages and disadvantages compared with traditional approaches that realise the same function.

***(10 marks)***

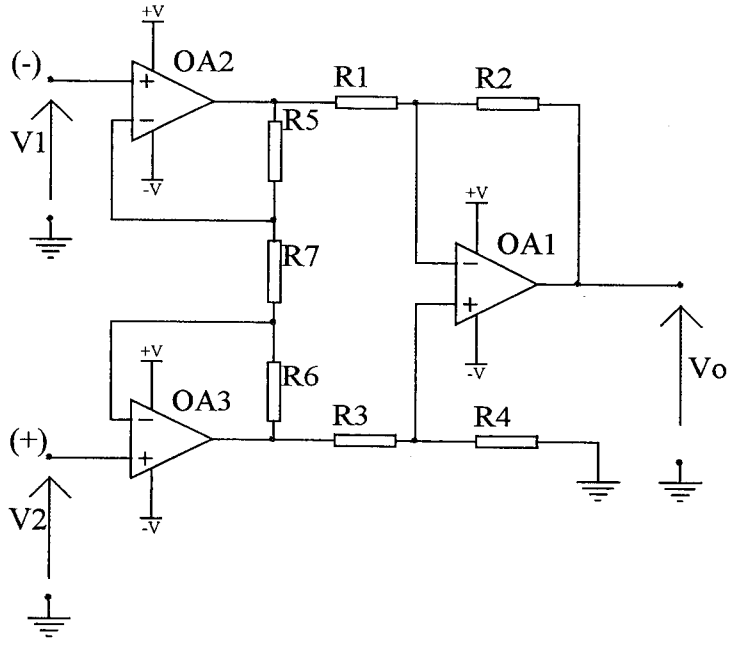



***Figure 3 (a)***

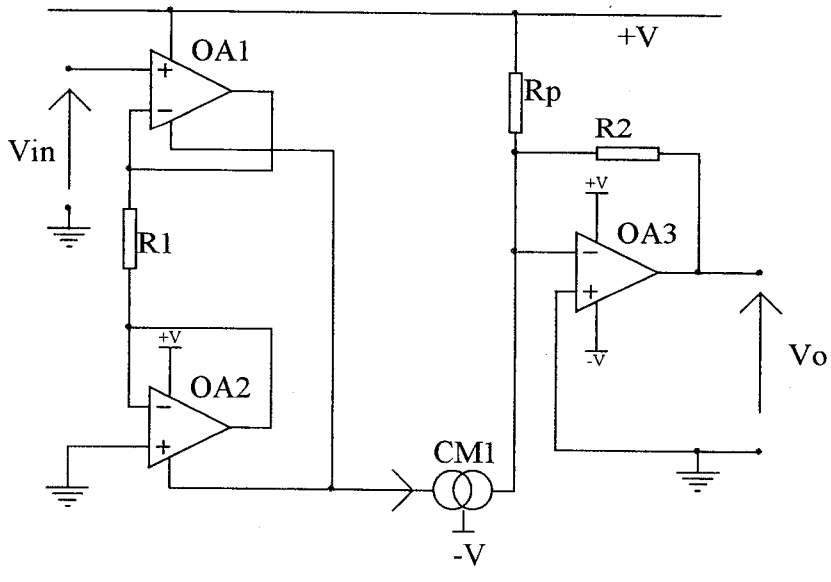



***Figure 3 (b)***

4. a) Derive the bipolar translinear principle with reference to a loop containing $2m$ base emitter junctions. State all the assumptions that you make, and list the conditions which must be satisfied in order for this principle to be valid.

***(4 marks)***

b) In addition, write down the MOS translinear principle for a loop of $V_{GS}$ junctions. Give three disadvantages of the MOS translinear principle compared to the bipolar version.

***(3 marks)***

c) *Figure 4a* shows a circuit containing a six transistor translinear loop.

i) Prove that this circuit implements a product/division function $I_{out} = \frac{I_X I_Y}{I_M}$.

ii) What is the condition that the current source $I_0$ should comply with for the circuit to operate properly?

iii) Show with the aid of a diagram how this circuit can be modified to implement the function $I_{out} = \frac{3}{2}\frac{I_X I_Y I_Z}{I_M I_N}$ with $I_Z$ and $I_N$ two additional currents.

***(8 marks)***

d) *Figure 4b* shows a circuit comprised of one translinear loop; $I_1$ and $I_3$ are input currents whereas $I_2$ and $I_4$ are constant bias currents. Derive an expression for the output current $I_{out}$ stating any assumptions that you make. What is the function of the circuit? What is the minimum value that should be selected for $I_2$ so that the circuit operates properly? Write down an expression for the output current:

i) when $I_1 = \left|\frac{dI_{in}}{dt}\right|$ and $I_3 = \left|\int I_{in}\, dt\right|$ and

ii) when $I_3 = \left|\frac{dI_{in}}{dt}\right|$ and $I_1 = \left|\int I_{in}\, dt\right|$.

In both cases $I_{in}(t) = A\sin(\omega t)$.

***(10 marks)***

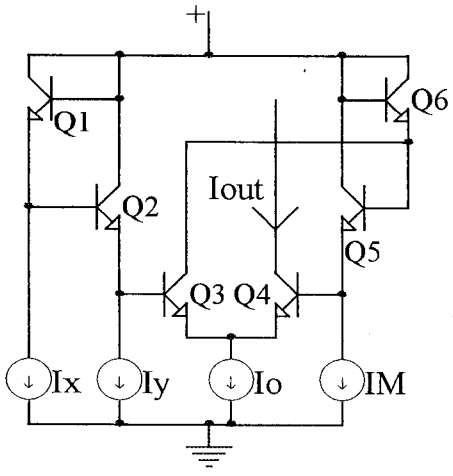



***Figure 4(a)***

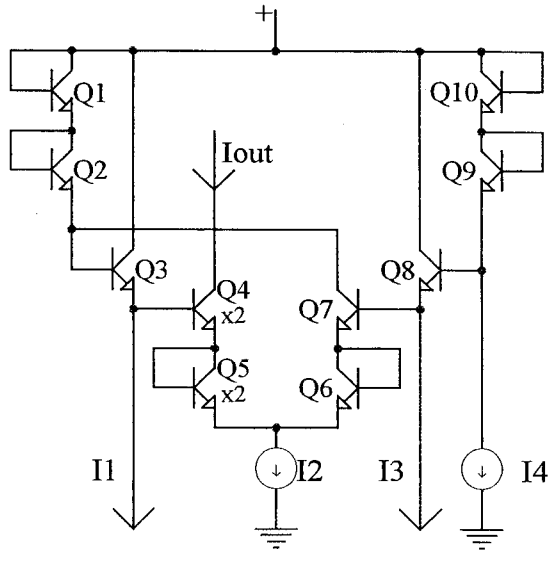



***Figure 4(b)***

5. a) *Figure 5* shows the general block diagram of a current-mode integrator where $f(\ )$ and $g(\ )$ represent non-linear functions. Derive an expression for the required relationship between $f(\ )$ and $g(\ )$ when the circuit of *Figure 5* operates as an input-output linear integrator, stating any assumptions that you make. Provided that the function $g(\ )$ in *Figure 5* is defined by $I_{out} = g(V_C) = \beta\,(V_C - V_{TH})^2$ (with $\beta$ being a constant of appropriate dimensions), derive an expression for the function $f(\ )$ to implement an input-output linear integrator.

***(6 marks)***

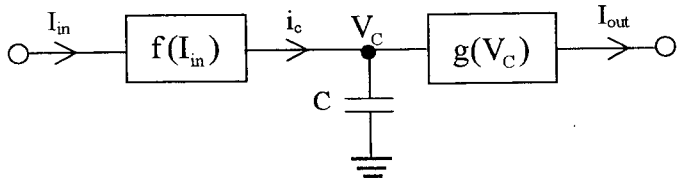



***Figure 5***

b) You are required to implement an oscillator with the following transfer function:

$T(s) = \dfrac{\omega_0^{\,2}}{s^2 + \omega_0^{\,2}}$. This transfer function can be decomposed into the following set of state-space equations:

$$\dot{x}_1 = -\omega_0 x_1 + \omega_0 x_2$$

$$\dot{x}_2 = -2\omega_0 x_1 + \omega_0 x_2 + \omega_0 U$$

$$y = x_1$$

$U$ is an input which is tuned to initially start an oscillation, $y$ is the output, whereas $x_1, x_2$ denote the state variables (a dot above a variable denotes time-differentiation). Using the exponential mappings $x_j = I_0 \exp(V_j/V_T)(j = 1,2)$, $U = I_S \exp(V_u/V_T)$ show that the above linear state-equations can be transformed into non-linear log-domain design equations.

***(8 marks)***

c) From these design equations and exploiting the known properties of the E+ and E- cells, sketch a transistor level implementation of the desired log-domain oscillator. Assuming that all capacitors are equal to *10pF* determine d.c. bias values to produce an oscillation frequency equal to $\omega_0 = 2\pi(20\times10^6)\,rad/s$ ($V_T \cong 26mV$).

***(11 marks)***

6. a) State the relationship which must be satisfied by two N-port networks, if these two networks are to be considered adjoint networks. Exploiting this relation derive the adjoint network of : (i) a resistor, (ii) a nullor and (iii) an open-loop 'ideal' voltage amplifier.

***(6 marks)***

b) You are required to implement the closed-loop *I-I* converter shown in *Figure 6a* by means of one of the four 'ideal' amplifiers.

i) State the four 'ideal amplifiers', their open-loop gain function and their ideal input and output impedances.

ii) Provided that the source and load impedances in *Figure 6a* are unknown, which of the four 'ideal amplifiers' you would choose in order to implement the block A? Justify your reasoning.

iii) Assuming that each of the 'ideal amplifiers' has ideal input and output impedance levels but finite open-loop gain and bandwidth, derive an expression for the frequency-dependent closed-loop gain of the configuration you have selected.

iv) Comment on both the advantage and the disadvantage of the configuration you have selected.

***(8 marks)***

c) *Figure 6b* shows the architecture of a simple current-follower where the symbols CM represent current mirrors with an arrow marking the input side.

i) Derive expressions for the d.c. input offset voltage and the small-signal input resistance at node X.

ii) Explain with the aid of a diagram how the circuit of *Figure 6b* can be modified to reduce the d.c. offset using additional diodes; comment on both the advantages and the disadvantages of this technique.

iii) Explain with the aid of a diagram how the circuit of *Figure 6b* can be modified to reduce the d.c. offset without increasing the input resistance.

***(11 marks)***

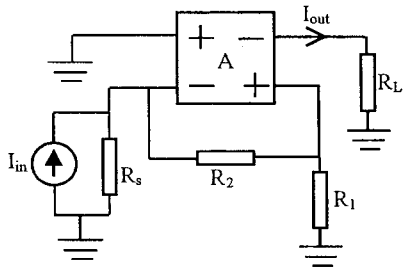



***Figure 6(a)***

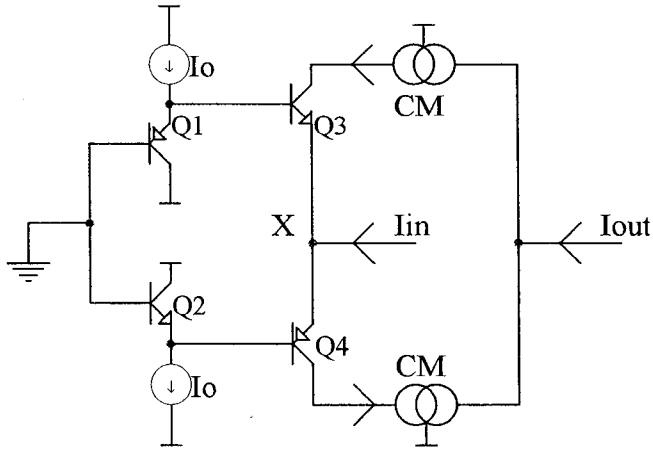
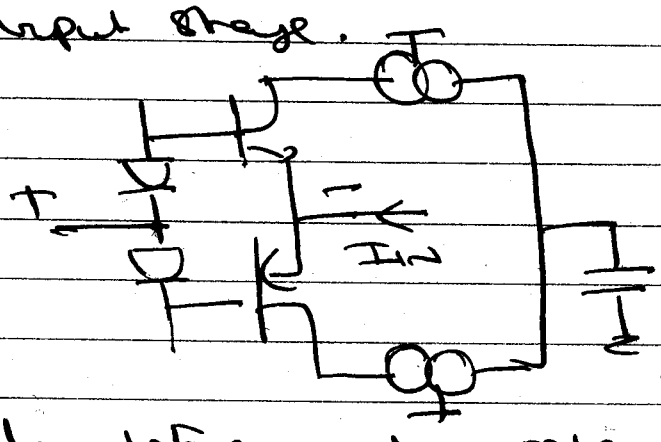



***Figure 6(b)***

# 4th Current-Mode - 2001 E4.16
# ANALOG Solutions Am 3

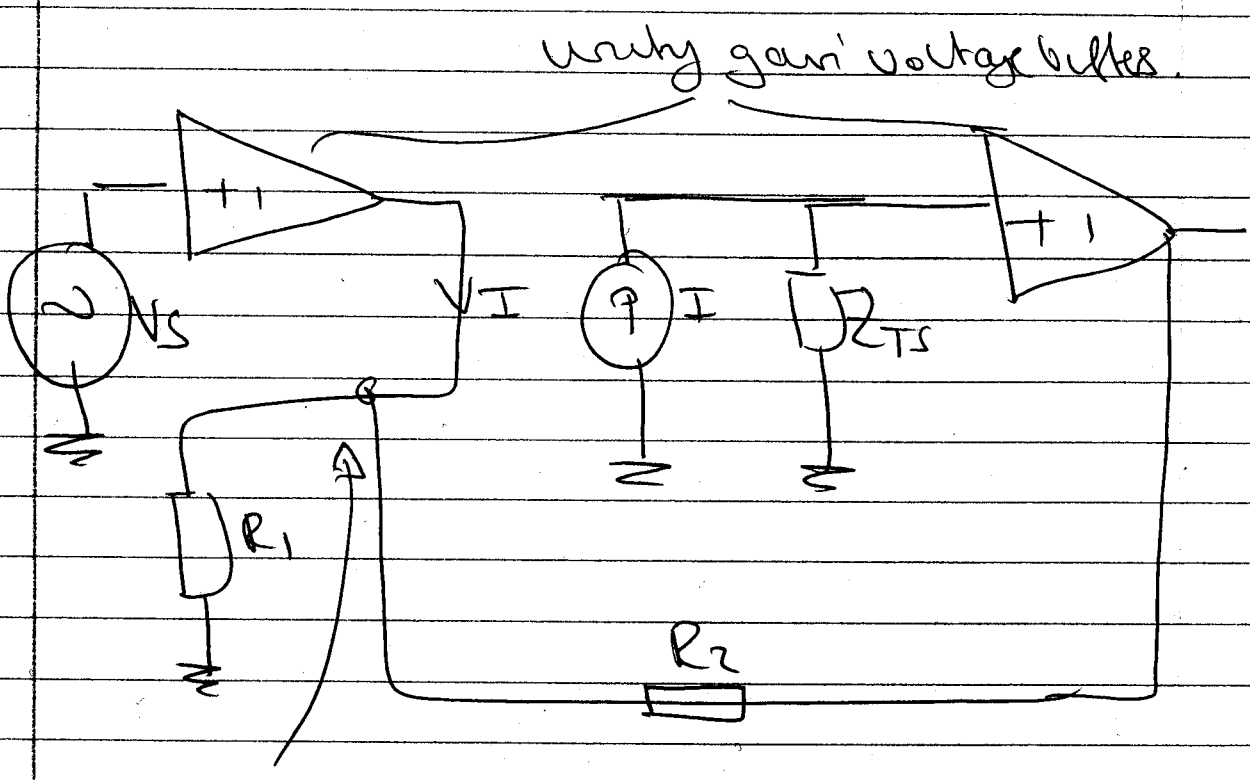
In two sections - each numbered out of 12 * (1)

(1) Transistors $Q_1$-$Q_4$ - quasi-class AB input stage - voltage follower. Current mirrors $Q_9$-$Q_{12}$, $Q_5$-$Q_8$ sense output buffer current and transfer to high impedance node Z creating high gain stage. Output buffer $Q_{13}$-$Q_{16}$ ensures required low impedance output. Current feedback is provided to the -ve input terminal via a feedback resistor R. The dominant pole of the amplifier is determined by the compensation capacitor C and the resistance at the Z-node. The closed loop bandwidth is determined by feedback resistor R and compensation capacitor C. Bias current $I_O$ does not limit the slew-rate as would be the case with the more classical long-tail pair input stage.




Assume $I_{IN}$ charges C giving a very high $I_{IN}/C = \frac{dv}{dt}$

Main limitation on slew-rate is the power supply limits and power rating of device. Potentially slew rates of the order of 1000V/μs possible with this type of op-amp. (6)

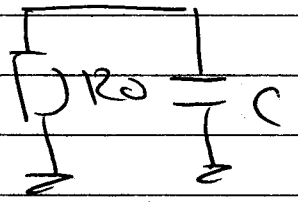



Current - feedback junction

Assume transimpedance form $Z_T(s) = V_o/I$

$= R_o/(1 + jf/f_p)$

where $f_p = 1/2\pi R_o C \Rightarrow$




from model $V_s/R_1 - \frac{(V_o - V_s)}{R_2}$

$= V_o/Z_T(s)$

$\therefore V_s/R_1 // R_2 = V_o/(Z_T(s) // R_2)$

OR $V_o/V_s = \frac{Z_T(s) // R_2}{R_1 // R_2}$

This gives $(V_o/V_s) = \frac{R_1 + R_2}{R_2}\left[\frac{Z_T}{R_2 + Z_T}\right]$

Sub in $Z_T(s)$

$V_o/V_s = \left[\frac{R_1 + R_2}{R_2}\right]\left(\frac{R_o}{R_o + R_2}\right)\left[\frac{1}{(1 + jf/f_p\frac{(R_o + R_2)}{R_2}}\right.$

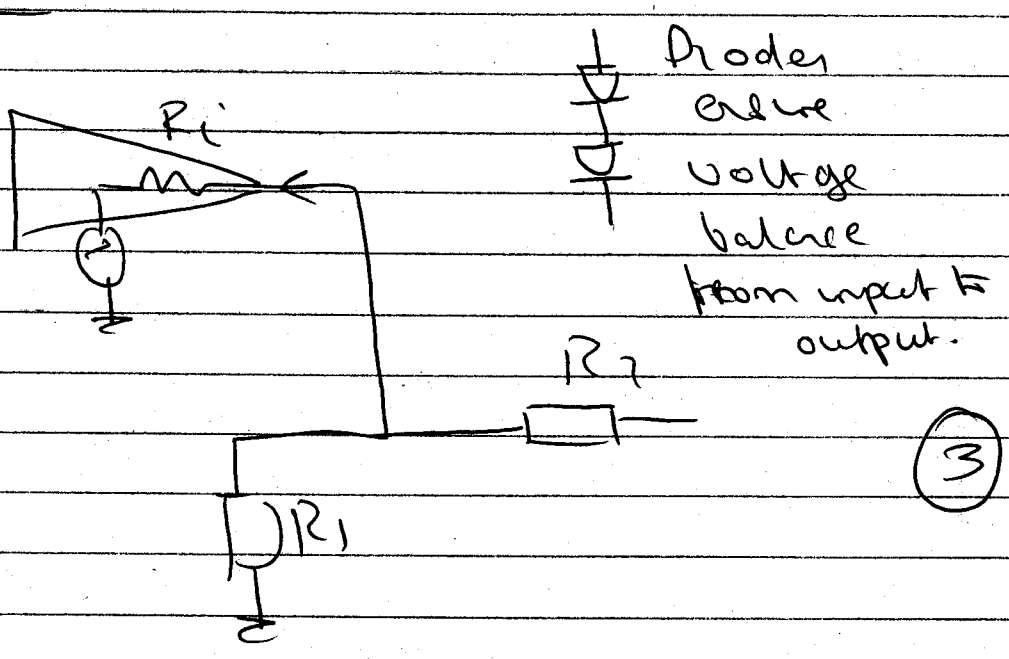
Assume

$R_0 \gg R_2$

then $f_p$ closed $= \frac{f_p R_0}{R_2} = \frac{1}{2\pi R_2 C}$

Closed loop gain $A_{c/c} = \left(\frac{R_1+R_2}{R_1}\right)$

Gain set by $R_1$, bandwidth by $R_2$. (7)




(3)

By considering $R_i$ of buffer then frequency gain expression

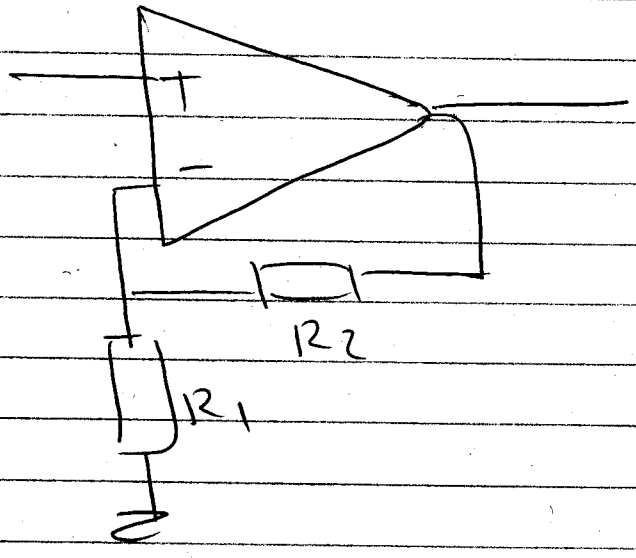
$f_p \simeq \frac{1}{2\pi(GR_i+R_2)C}$

∴ if $R_i = 0$ same as before (5)

if G large then $GR_i$ dominates.

and $f_p = \frac{1}{2\pi GR_iC} \Rightarrow$ Gain bandwidth product.

(D) 1 Cont




$$10\,MHz = \frac{1}{2\pi R_2 \times 4pF}$$

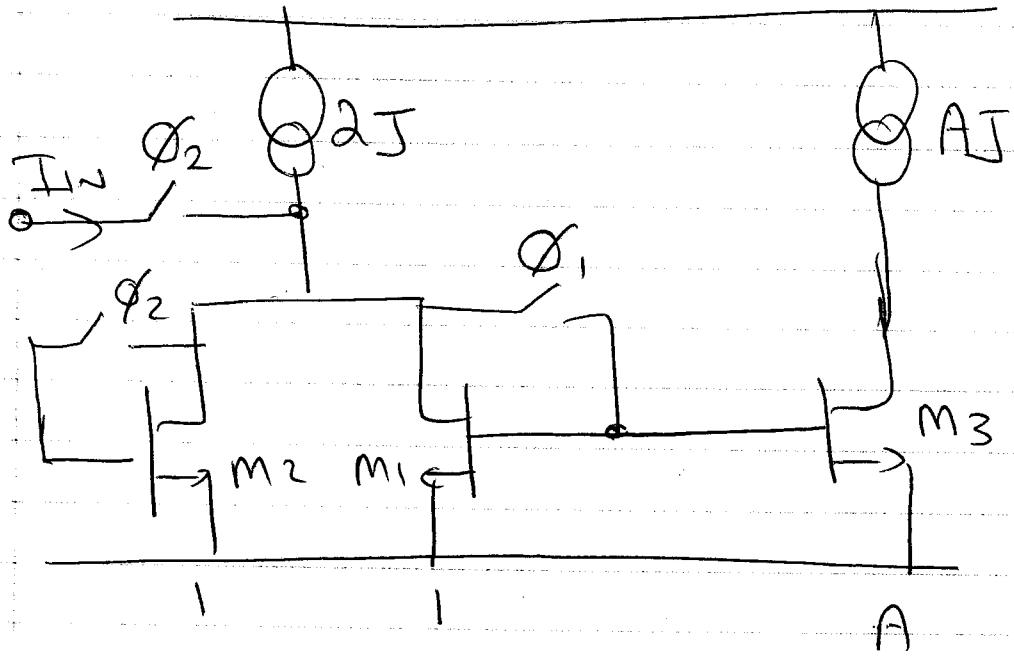
$R_2 = 10 R_1$

$\therefore R_2 =$

and so $R_1 =$ — (4)

TOTAL 25/25.

Qu 2.




$Q_2(n-1)$

$$I_{ds2_{(n-1)}} = (2J) + I_{in}(n-1) - I_{ds}(n-1)$$

$$= J + I_{in}(n-1) + \frac{I_o(n-1)}{A}$$

$\phi_2(n)$

$$I_{ds1}(n) = J - I_{in}(n-1) - \frac{I_o(n-1)}{A}$$

$$I_o(n) = A I_{in}(n-1) + I_o(n-1)$$

$$\therefore \quad I_o(1-z^{-1}) = A I_{in} z^{-1}$$

$$\therefore \quad \left(\frac{I_o}{I_{in}}\right)_z = \frac{Az^{-1}}{(1-z^{-1})}$$

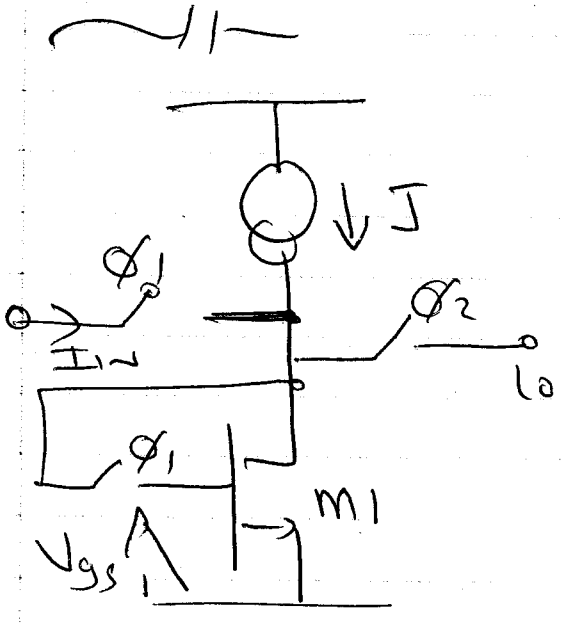
Since $z = e^{sT}$

When $\frac{I_O}{I_{IN}} = \frac{A}{2^1 - 1} \approx \frac{A}{e^{ST} - 1}$

for $ST \ll 1 \Rightarrow \frac{I_O}{I_{IN}} = \frac{A}{(1 + ST - 1)} = \frac{1}{ST/A}$

Hence time constant

$\tau = T/A$ — (10)

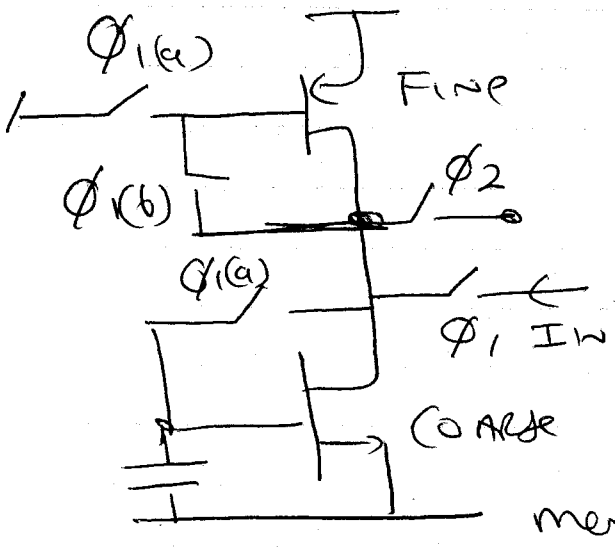



1/ Drain voltage variation (use regulated cascode)

2/ Charge injection error (dummy switches)

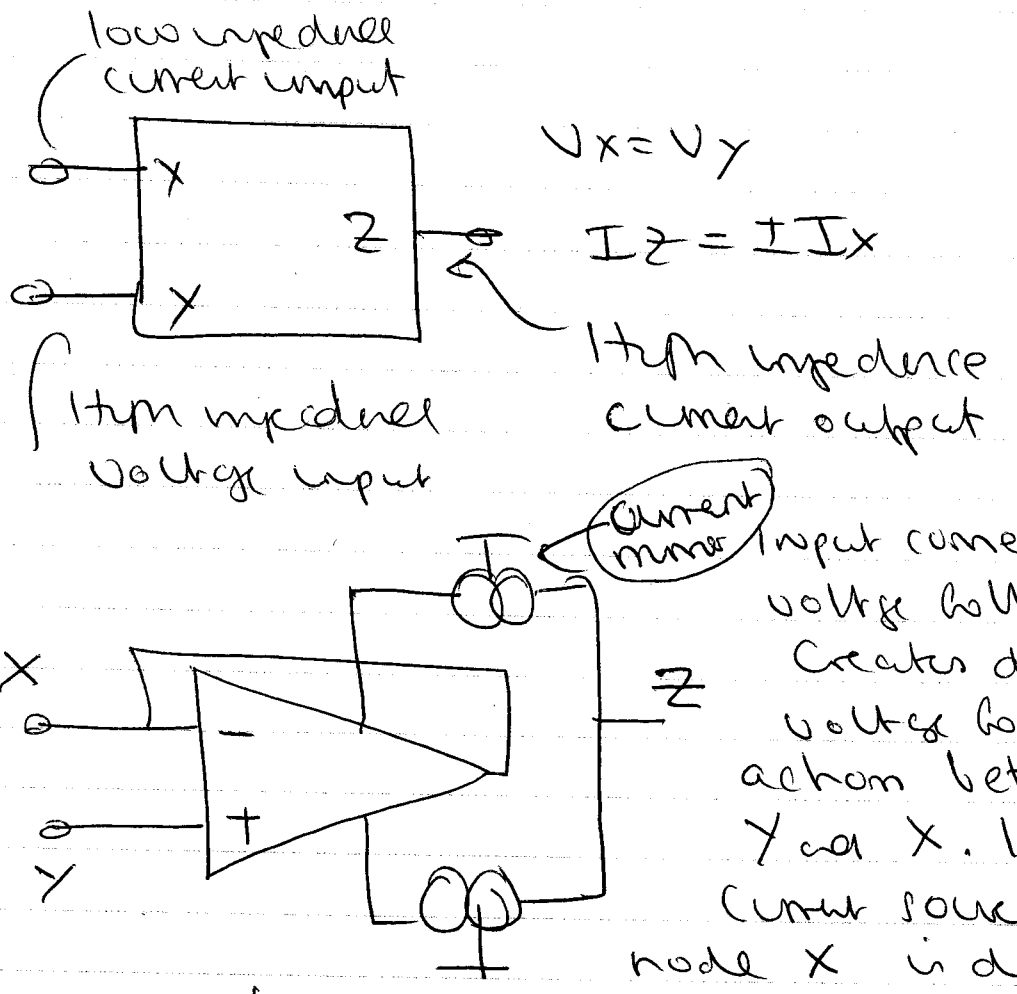
3/ settling-time error (smaller $C_P$)

4/ Signal swing (use CLASS AB) (2)




Two step approach eliminates most of the transistor errors.

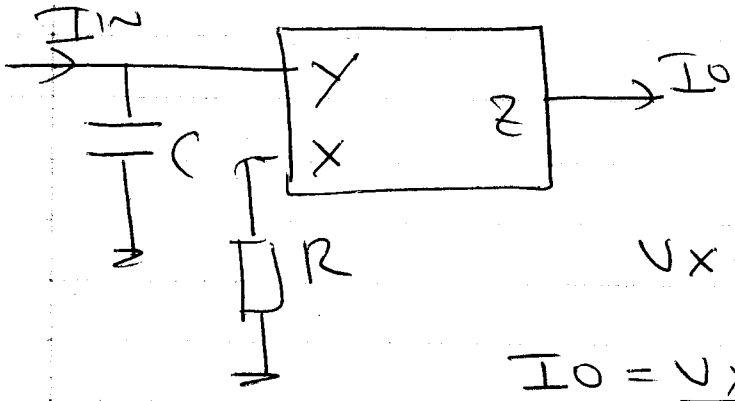
Errors are summed during $\phi_{1(b)}$ in the memory cell and then inverted at output during $\phi_2$




drawn by the output of the op-amp via the feedback loop and is forced into the negative power supply. This input current modulates the supply bus current and the total current is mirrored to the high impedance node (Z). (collector connection of current-mirror).

High bandwidth potential because op-amp is connected as a unity gain buffer. Also when ~~X~~ terminal connected to ground then the op-amp is enclosed in a 'ground'/'virtual ground' environment leading to high speed potential.

(10)




(3)

$$V_X = I_{IN}/sC$$

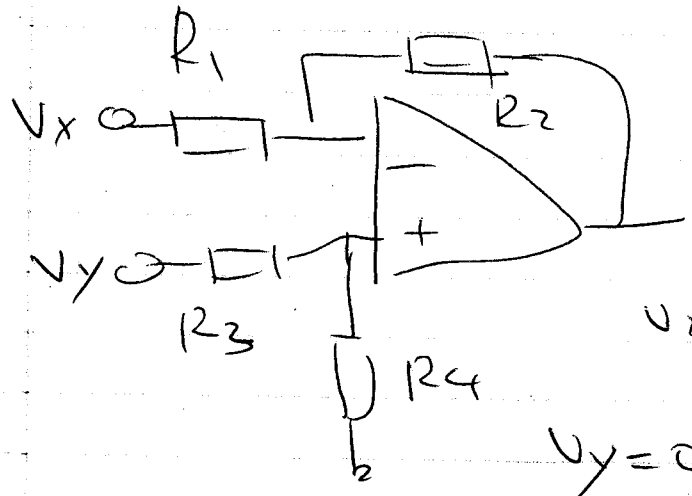
$$I_O = \frac{V_X}{R} = I_{IN}/sCR$$

$$I_O/I_{IN} = 1/sCR \rightarrow \underline{\text{Integrator}}$$

Change R and C to create a differentiator.

TOTAL 25/25

Qu 3 – Consider output stage




Superposition

$V_x = 0, \quad \frac{V_o}{V_y} = \left(1+\frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3+R_4}\right)$

$V_y = 0, \quad \frac{V_o}{V_x} = -\frac{R_2}{R_1}$

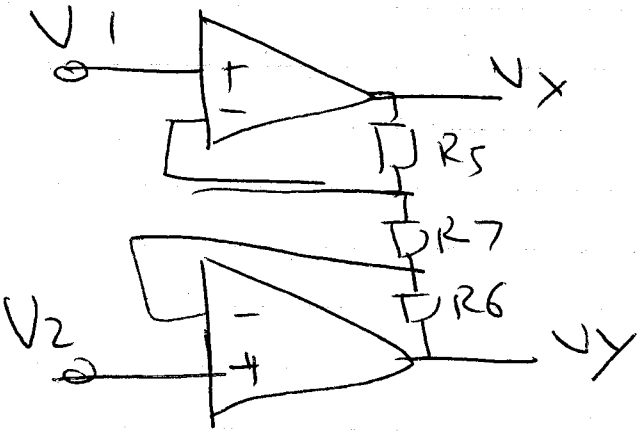
$\therefore V_o = \left[1+\frac{R_2}{R_1}\right]\left[\frac{R_4}{R_3+R_4}\right]V_y - \left(\frac{R_2}{R_1}\right)V_x$

If $\frac{R_2}{R_1} = \frac{R_4}{R_3}$ then $V_o = \frac{R_2}{R_1}\left[V_y - V_x\right]$

Choose $R_2 = R_4$, $R_3 = R_1$ to satisfy above also helps to minimize offsets due to input bias. Since $R_2 = R_4 = NR$

$R_1 = R$ then $V_o = N[V_y - V_x]$ – (2)

Pre-amp




$V_x = V_1 + (V_2 - V_1)R_5/R_7$

$V_y = V_2 + (V_2 - V_1)R_6/R_7$

$(V_y - V_x) = (V_2 - V_1)\left[1 + \frac{R_5}{R_7} + \frac{R_6}{R_7}\right]$

Assuming

$R_5 = R_6 = nR$
$R_7 = R$

$\Big\} (V_2 - V_1)[1+2m]$

∴ Complete Amp — Precision to reject diff sign and comm

$$V_o = (V_2 - V_1) N [1+2m]$$

Relys upon matching to yield low comm-mode gain — (3)

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Effect of mismatch

CMRR = ∞ , if $\frac{R_2}{R_1} = \frac{R_4}{R_3}$

$$V_o = \underbrace{\left(1+\frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3+R_4}\right)}_{k_2} V_y - \underbrace{\frac{R_2}{R_1}}_{k_1} V_x$$

$$V_o = k_2 V_y - k_1 V_x$$

If $V_y = V_x = V_{cm} \Rightarrow A_{cm} = V_o/V_{cm} = (k_2 - k_1)$

If $V_y = \frac{V_d}{2}$ and $V_x = -V_d/2$

$$\Rightarrow A_d = V_o/V_d = \left(\frac{k_2+k_1}{2}\right)$$

$$\therefore CMRR = Ad/Acm = \frac{(k_2+k_1)}{2(k_2-k_1)} \quad \text{--- (2)}$$

Consider tolerance

$$R_1 = R(1+\delta_1), \quad R_2 = NR(1+\delta_2)$$

$$R_3 = R(1+\delta_3) \quad R_4 = NR(1+\delta_4)$$

Sub, $R_1$ to R4 into (2) given

$$CMRR = \frac{1}{2}\left[\frac{R_1R_4 + 2k_2R_4 + R_2R_3}{R_1R_4 - R_2R_3}\right]$$

$$= \frac{(1+N)}{(\delta_1+\delta_4) - (\delta_2+\delta_3)}$$

when $\delta$ accumulates maximum value $= 4t$ where $t$ = tolerance

for $m = N = 1$ (8)

Hence $\frac{CMRR \text{ of}}{\text{Compare Amp}} = \frac{(1+2m)(1+N)}{4t}$

for $m = N = 1 \Rightarrow CMRR = (1.5/t)$ (16/15)

The circuit of Figure 3(b) is a current mode precision rectifier.

For $V_{IN} > 0$, input current of $(V_{IN}/R_1)$ is drawn from +ve supply of OA1 and negative supply of OA2.

For $V_{IN} < 0$, input current of $V_{IN}/R_1$ is drawn from negative supply of OA1 and positive supply of OA2.
In both phases the current through the negative supply of OA1 and OA2 is summed at the input of current mirror CM1. Therefore the power supplies of the op-amp are being used to rectify the signal current.
Hence a positive current of $V_{IN}/R_1$ will always appear at the input of CM1 irrespective of the sign of $V_{IN}$.
The net summed current is then mirrored to the output transimpedance amplifier OA3/R and converted back to a voltage. Thus $V_O = -R_2/R_1 | V_{IN}|$
Rp - trimming resistor.

Advantages :- No diodes
- No non-linear distortion
- Op-amps always closed loop, no slewrate problems at low frequency.

10/6

TOM 25/2/5

④ • Equal number of CW & ACW npn junctions
• Equal number of CW & ACW pnp junctions
• All devices have same $V_T$ (ie, same temp.)
• All npn (pnp) devices have same current density $J_{Sn}$ ($J_{Sp}$) :

$$CW \sum_{j=1}^{m} V_{BEj} = ACW \sum_{j=1}^{m} V_{BEj}$$

$$CW \sum_{j=1}^{m} V_T \ln\left(\frac{I_{Cj}}{J_{Sj} A_j}\right) = ACW \sum_{j=1}^{m} V_T \ln\left(\frac{I_{Cj}}{J_{Sj} A_j}\right)$$

$$CW \prod_{j=1}^{m} \left(\frac{I_{Cj}}{J_{Sj} A_j}\right) = ACW \prod_{j=1}^{m} \left(\frac{I_{Cj}}{J_{Sj} A_j}\right)$$

$$\therefore \; CW \prod_{j=1}^{m} \left(\frac{I_{Cj}}{A_j}\right) = ACW \prod_{j=1}^{m} \left(\frac{I_{Cj}}{A_j}\right)$$

BIPOLAR TRANSLINEAR PRINCIPLE ④

MOS TRANSLINEAR PRINCIPLE:

$$CW \sum_{j=1}^{m} \sqrt{\frac{I_{Dj}}{K_j}} = ACW \sum_{j=1}^{m} \sqrt{\frac{I_{Dj}}{K_j}}$$

$$K_j = \mu C_{ox} \frac{W}{2L}$$

Disadvantages: 'Sum of roots' relation is not as widely useful as bipolar TL 'products'

: MOS square law is valid over a smaller current range
: process parameters ($\mu$) do not automatically cancel for 'mixed' (NMOS & PMOS) TL loops.

(3)

(i) Fig 4a:

$$I_{C1} \cdot I_{C2} \cdot I_{C3} = I_{C4} \cdot I_{C5} \cdot I_{C6}$$

$I_{C1} = I_X$ $\quad I_{C2} = I_Y$ $\quad I_{C3} = I_O - I_{OUT}$
$I_{C4} = I_{OUT}$ $\quad I_{C5} = I_M$ $\quad I_{C6} = I_{C3} = I_O - I_{OUT}$

$$\Rightarrow I_X \cdot I_Y \cdot (I_O - I_{OUT}) = I_{OUT} \cdot I_M \cdot (I_O - I_{OUT})$$

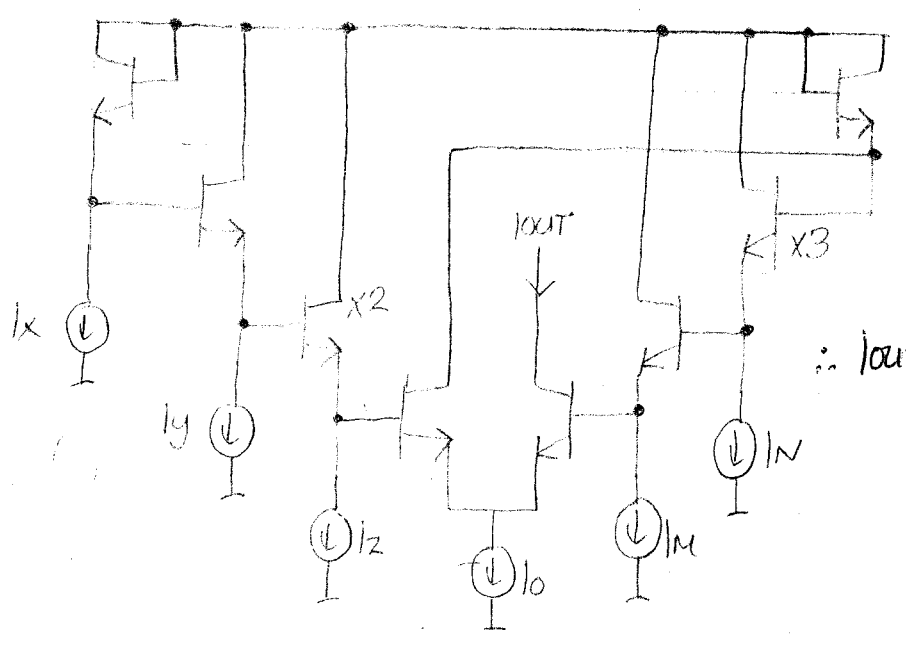
$$I_{OUT} = \frac{I_X \cdot I_Y}{I_M}$$

(2)

(ii) In order for Q3 & Q6 to remain biased, $I_O - I_{OUT} > 0$, thus $I_O > I_{OUT(MAX)}$

(2)

iii) Modified circuit: $I_X \cdot I_Y \cdot \frac{I_Z}{2} \cdot (I_O - I_{OUT}) = I_{OUT} \cdot I_M \cdot \frac{I_N}{3} (I_O - I_{OUT})$




$$\therefore I_{OUT} = \frac{3 I_X I_Y I_Z}{2 I_M I_N}$$

(4)

4b)

$$I_{C1} \cdot I_{C2} \cdot I_{C3} \cdot \frac{I_{C4}}{2} \cdot \frac{I_{C5}}{2} = I_{C6} \cdot I_{C7} \cdot I_{C8} \cdot I_{C9} \cdot I_{C10}$$

Assuming base currents can be neglected.

$I_{C1} = I_{C2} = (I_2 - I_{OUT})$
$I_{C3} = I_1$
$I_{C4} = I_{C5} = I_{OUT}$
$I_{C6} = I_{C7} = (I_2 - I_{OUT})$
$I_{C8} = I_3$
$I_{C9} = I_{C10} = I_4$

$$\therefore \quad (I_2 - I_{OUT})^2 I_1 \cdot \frac{I_{OUT}^2}{4} = (I_2 - I_{OUT})^2 I_3 \cdot I_4^2$$

$$I_{OUT}^2 = \frac{4 \cdot I_3 I_4^2}{I_1}$$

$$I_{OUT} = 2 I_4 \cdot \sqrt{\frac{I_3}{I_1}}$$

(4)

To ensure Q1 / Q2 / Q6 / Q7 are correctly biased,

$$I_2 > I_{OUT(max)}$$

(2)

$I_{in}(t) = A \sin(\omega t)$

$\left| d I_{in}/dt \right| = A\omega \cos(\omega t)$

$\left| \int I_{in}\, dt \right| = \frac{A}{\omega} \cos(\omega t)$

i) $I_{OUT} = 214 \cdot \sqrt{\dfrac{\frac{A}{\omega} \cdot \cos\omega t}{A\omega \cos\omega t}} = \dfrac{214}{\omega}$ (2)

ii) $I_{OUT} = 214 \sqrt{\dfrac{A\omega \cos\omega t}{\frac{A}{\omega} \cos\omega t}} = 214 \cdot \omega$ (2)

TOTAL = (25)

⑤ $I_C = f(I_{in})$ & $I_{OUT} = g(V_C)$

Assuming input impedance of block $g(\,)$ is infinite.

$$I_{OUT} = g(V_C)$$

$$\frac{dI_{OUT}}{dt} = \frac{dg(V_C)}{dV_C}\cdot\frac{dV_C}{dt} = \frac{dg(V_C)}{dV_C}\cdot\frac{I_C}{C} = \frac{dg(V_C)}{dV_C}\cdot\frac{f(I_{in})}{C}$$

For an input-output linear integrator

$$\frac{dI_{out}}{dt} = \frac{I_{in}}{\tau}$$

Thus $$\frac{I_{in}}{\tau} = \frac{dg(V_C)}{dV_C}\cdot\frac{f(I_{in})}{C}$$

or $$f(I_{in}) = \frac{I_{in}\cdot C}{\tau}\left(\frac{dg(V_C)}{dV_C}\right)^{-1}$$ (3)

$$I_{OUT} = g(V_C) = \beta(V_C - V_{TH})^2$$

$$\frac{dg(V_C)}{dV_C} = 2\beta(V_C - V_{TH}) = 2\sqrt{\beta I_{OUT}}$$

Thus $$I_C = f(I_{in}) = \frac{I_{in}\,C}{\tau\cdot 2\sqrt{\beta I_{OUT}}} = I_{in}\cdot\sqrt{\frac{I_0}{I_{OUT}}}$$

where $$I_0 = \left\{\frac{C}{2\tau\sqrt{\beta}}\right\}^2$$ (3)

Oscillator

$$\dot{x}_1 = -\omega_0 x_1 + \omega_0 x_2$$
$$\dot{x}_2 = -2\omega_0 x_1 + \omega_0 x_2 + \omega_0 u$$
$$y = x_1$$

$$x_1 = I_0 \exp(V_1/V_T) \qquad \dot{x}_1 = \frac{x_1}{V_T}\cdot \dot{V}_1$$

$$x_2 = I_0 \exp(V_2/V_T) \qquad \dot{x}_2 = \frac{x_2}{V_T}\cdot \dot{V}_2$$

$$u = I_s \exp(V_u/V_T)$$

$$\Rightarrow \dot{V}_1 (x_1/V_T) = -\omega_0 x_1 + \omega_0 x_2$$
$$\dot{V}_2 (x_2/V_T) = -2\omega_0 x_1 + \omega_0 x_2 + \omega_0 u$$
$$y = x_1$$

$$\Rightarrow C\dot{V}_1 = -C\omega_0 V_T + C\omega_0 V_T (x_2/x_1)$$
$$C\dot{V}_2 = -2C\omega_0 V_T (x_1/x_2) + C\omega_0 V_T + C\omega_0 V_T (u/x_2)$$
$$y = x_1$$

$$\Rightarrow C\dot{V}_1 = -I_0 + I_0 \exp\left(\frac{V_2 - V_1}{V_T}\right)$$

$$C\dot{V}_2 = -2I_0 \exp\left(\frac{V_1 - V_2}{V_T}\right) + I_0 + I_S \exp\left(\frac{V_u - V_2}{V_T}\right)$$

$$y = I_0 \exp \frac{V_1}{V_T}$$

where $I_0 = C\omega_0 V_T$

Define $I_0 = I_S \exp(V_0/V_T)$

$$\Rightarrow C\dot{V}_1 = -I_0 + I_S \exp\left(\frac{V_2 + V_0 - V_1}{V_T}\right)$$

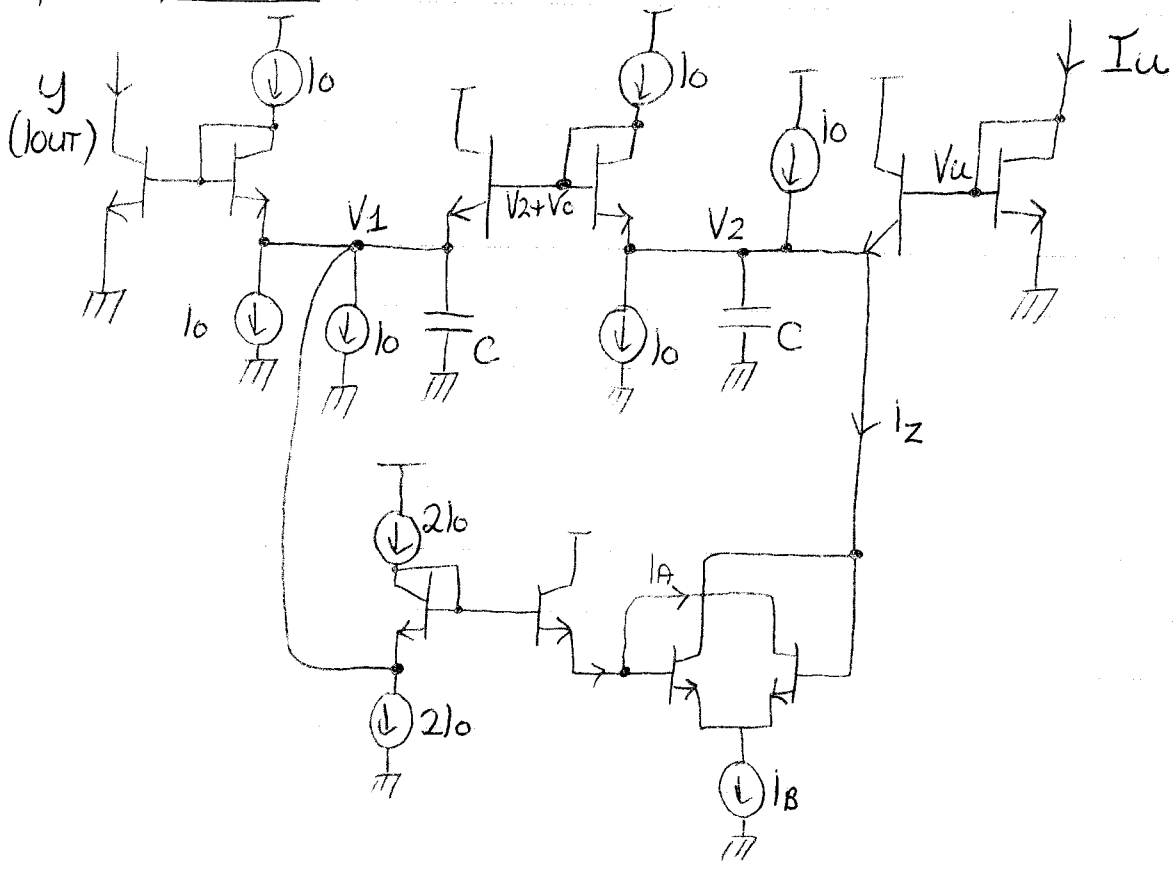
$$C\dot{V}_2 = -2I_0 \exp\left(\frac{V_1 - V_2}{V_T}\right) + I_0 + I_S \exp\left(\frac{V_u - V_2}{V_T}\right)$$

$$y = I_S \exp\left(\frac{V_1 + V_0}{V_T}\right)$$

(8)

$$V_u = V_T \ln(I_u/I_S)$$

Implementation:




(9)

$$V_1 + V_T \ln(2I_0/I_S) - V_T \ln(I_A/I_S) - V_T \ln(I_z/I_S) + V_T \ln(I_A/I_S) = V_2$$

$$(V_1 - V_2) = V_T \ln(I_z/2I_0)$$

$$I_z = 2I_0 \exp(V_1 - V_2)/V_T \quad \text{as required}$$

$$\omega_0 = 2\pi(20 \times 10^6) = I_0/CV_T$$

$$I_0 = 2\pi(20 \times 10^6) \cdot 10p \cdot 25mV$$

$$= 31.2\,\mu A$$

(2)

TOTAL = (25)

6. Two N-port networks are adjoint elements if

$$\sum_{n=1}^{N} \left\{ V_n^A I_n^B - I_n^A V_n^B \right\} = \emptyset$$

where 'A' refers to the first network, and 'B' refers to the second. (1)

(i) A resistor is a 2 port element with $V^A, I^A$, where $V^A / I^A = R$

$$\Rightarrow \quad V^A \cdot I^B - I^A V^B = \emptyset$$
$$V^A I^B = I^A V^B$$
$$\frac{V^A}{I^A} = \frac{V^B}{I^B} = R$$

(1)

$\therefore$ Adjoint element $V^B, I^B$ is also a resistor of value $R$.

(ii) Nullor is a 2 port element with $V_1^A = \emptyset$, $I_1^A = \emptyset$, $V_2^A = X$, $I_2^A = X$ ($X$ = undefined)

$$V_1^A I_1^B - I_1^A V_1^B + V_2^A I_2^B - I_2^A V_2^B = \emptyset$$
$$0 \cdot I_1^B - 0 \cdot V_1^B + X \cdot I_2^B - X \cdot V_2^B = \emptyset$$

$\therefore$ $I_2^B$ & $V_2^B$ must be zero, $I_1^B$ & $V_1^B$ can be $X$ } to ensure condition is always satisfied.

Adjoint element has $V_2^B, I_2^B = \emptyset$ & $V_1^B, I_1^B = X$.
i.e. it is a nullor with input & output ports interchanged. (2)

iii) Ideal open loop voltage amp

$$V_1^A = V_{in}, \quad I_1^A = \emptyset, \quad V_2^A = A \cdot V_{in}, \quad I_2^A = X$$

Thus:

$$V_{in} \cdot I_1^B - 0 \cdot V_1^B + A V_{in} I_2^B - X \cdot V_2^B = \emptyset$$

$$V_2^B = \emptyset \quad (\text{since } I_2^A = X)$$

$$\Rightarrow V_{in} \cdot I_1^B + A \cdot V_{in} I_2^B = \emptyset$$

$$\therefore I_1^B = A \cdot I_2^B$$

The adjoint network:

$$V_2^B = \emptyset, \quad I_2^B = I_{in}, \quad V_1^B = X, \quad I_1^B = A \cdot I_{in}$$

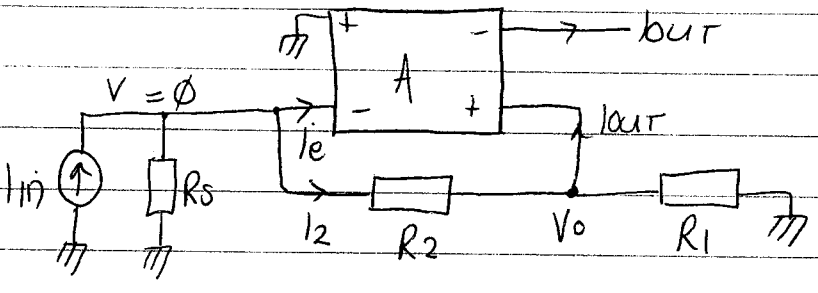
Current amplifier with port 2 as input & port 1 as output. (2)

Fig. 6a.

(i) Voltage amp: o/c voltage gain, $R_{in} = \infty$, $R_{out} = \emptyset$
Current amp: o/c current gain, $R_{in} = \emptyset$, $R_{out} = \infty$
Transresistance amp: o/c transresistance gain, $R_{in} = R_{out} = \emptyset$
Transconductance amp: o/c transconductance gain, $R_{out} = R_{in} = \infty$ (2)

(ii) Current amplifier should be chosen, since this is the only amp with the necessary input & output impedance levels to ensure that the resulting closed-loop TF is independent of $R_S$ & $R_L$. (2)

(iii)



$$I_{in} = I_e + I_2 = \frac{I_{OUT}}{A} - \frac{V_o}{R2}$$

$$I_{OUT} = \frac{-V_o}{R_2} - \frac{V_o}{R_1} = -V_o\frac{(R_1+R_2)}{R_1R_2}$$

$$I_{IN} = \frac{I_{OUT}}{A} + \frac{I_{OUT}}{R_2}\left(\frac{R_1R_2}{R_1+R_2}\right)$$

$$\frac{I_{OUT}}{I_{IN}} = (1+R_2/R_1)\left\{\frac{A}{A+(1+R_2/R_1)}\right\}$$

$$A = \text{o/c gain} = \frac{A_0}{1+S/\omega_0} \simeq \frac{A_0\omega_0}{S} = \frac{GB}{S}$$

$$\Rightarrow \frac{I_{OUT}}{I_{IN}} = (1+R_2/R_1)\left\{\frac{1}{1+SGB/(1+R_2/R_1)}\right\} \quad (2)$$

Advantage: C/L bandwidth is independent of $R_S$ & $R_L$, thus B/W remains stable as source & load vary

Disadvantage: C/L bandwidth is inversely proportional to gain ie a fixed gain-bandwidth conflict (2)

Figure 6b.

(i) when $I_{in} = \emptyset$, $I_{C3} = I_{C4}$

By TLP: $I_{C1} \cdot I_{C2} = I_{C3} \cdot I_{C4}$

$I_o^2 = I_{C3} \cdot I_{C4}$ $\quad I_{C3} = I_{C4} = I_o$

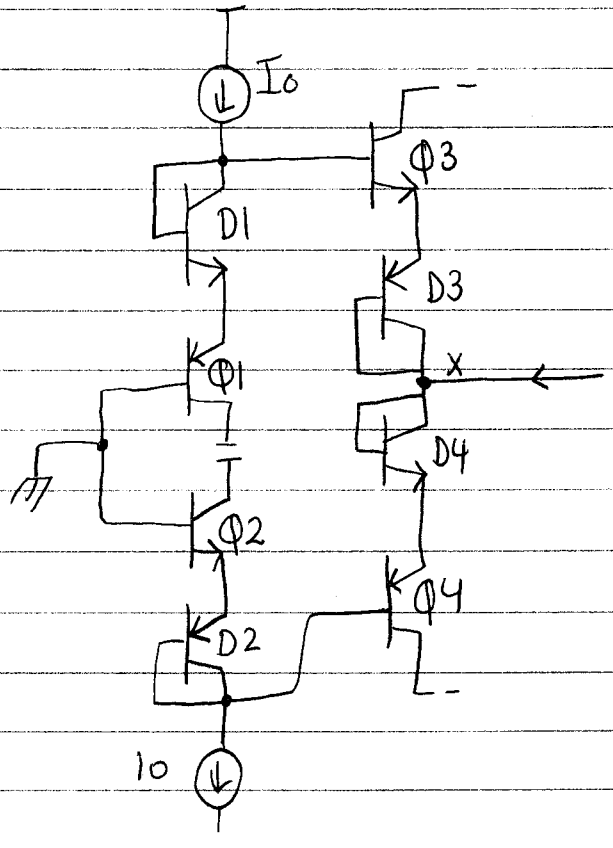
$$V_X = V_{BE1} - V_{BE3}$$
$$= V_T \ln\left(\frac{I_o}{I_{SP}} \frac{I_{SN}}{I_o}\right) = V_T \ln\left(\frac{I_{SN}}{I_{SP}}\right)$$

DC (QUIESCENT) OFFSET VOLTAGE $= V_T \ln\left(\frac{I_{SN}}{I_{SP}}\right) \neq 0.$

SMALL SIGNAL INPUT RESISTANCE $r_X \simeq r_{e3} // r_{e4}$

$$\approx \frac{V_T}{2I_o} \qquad (2)$$

(ii) Reduce dc offset using diodes:



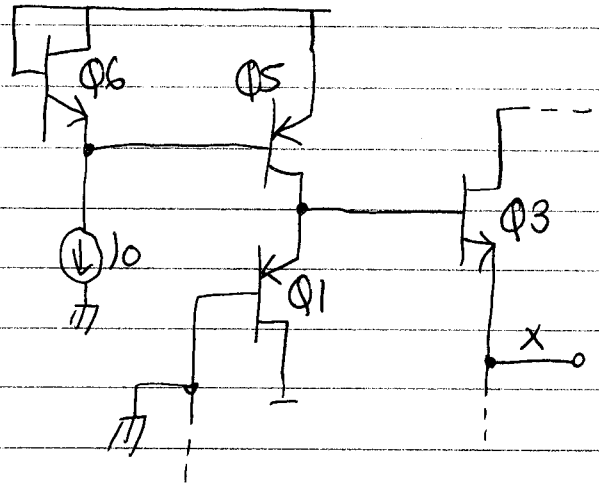
In absence of any signal, all devices have current $I_o$:

$$V_x = V_{be1} + V_{d1} - V_{be3} - V_{d3}$$
$$= V_T \ln\left(\frac{I_o}{I_{sp}} \cdot \frac{I_o}{I_{sn}} \cdot \frac{I_{sn}}{I_o} \cdot \frac{I_{sp}}{I_o}\right) = V_T \ln(1) = 0$$ (3)

Advantages: offset is reduced to zero by relying on matching between 'like' devices.
Disadvantages: Small-signal input resistance $r_x$ is ≃ doubled. We also need a higher supply voltage. (2)

(iii) Reducing dc offset without increasing $r_x$ (or $I_o$!):

use scaled current sources




$$V_{be6} = V_T \ln(I_o/I_{sn}) = V_{be5}$$

$$I_{c5} = I_s \cdot \exp(V_{be5}/V_T) = I_{sp} \exp(\ln[I_o/I_{sn}])$$
$$= I_{sp} \cdot I_o / I_{sn}$$

$I_{c1} = I_{c5}$, thus $V_{be1} = V_T \ln(I_{c5}/I_{sp})$ (4)
$= V_T \ln(I_o/I_{sn})$

Q1 'looks' like an npn, thus will match Q3!

TOTAL = (25)