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Paper Number(s): **E4.16**
AM3

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2000

MSc and EEE PART IV: M.Eng. and ACGI

CURRENT-MODE ANALOGUE SIGNAL PROCESSING

Thursday, 11 May 2000, 10:00 am

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks.

Corrected Copy

Time allowed: 3:00 hours

Q. 5.

Examiners: Prof C. Toumazou, Dr A.J. Payne, Dr C. Papavassiliou

Special instructions for invigilators: None

Information for candidates: None

1. (a) Advanced bipolar technology has led to the development of a new generation of high-speed 'current-mode' analogue building blocks: the current-feedback op-amp and the current conveyor. With the aid of a suitable current-feedback amplifier macro-model, show how constant-bandwidth amplification is obtained in EITHER of these designs.

[13 marks]

(b) The circuit shown in *Figure 1(a)* is network symbol of a second-generation current conveyor. Describe the terminal relationships of the current conveyor, and explain why the device is so versatile. [4 marks]

(c) An implementation of the current-conveyor is shown in *Figure 1(b)*. Explain how the circuit works and why it can achieve a slew-rate higher than that of a classical voltage operational amplifier. Explain why transistors Q_5 – Q_8 help to significantly reduce offset voltage between node Y and X. [8 marks]

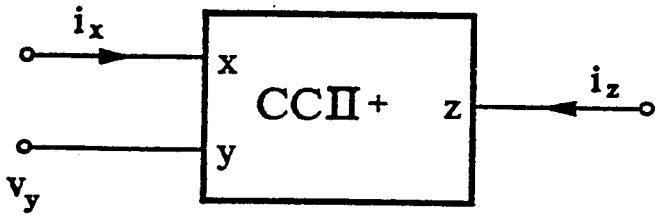


Figure 1(a)

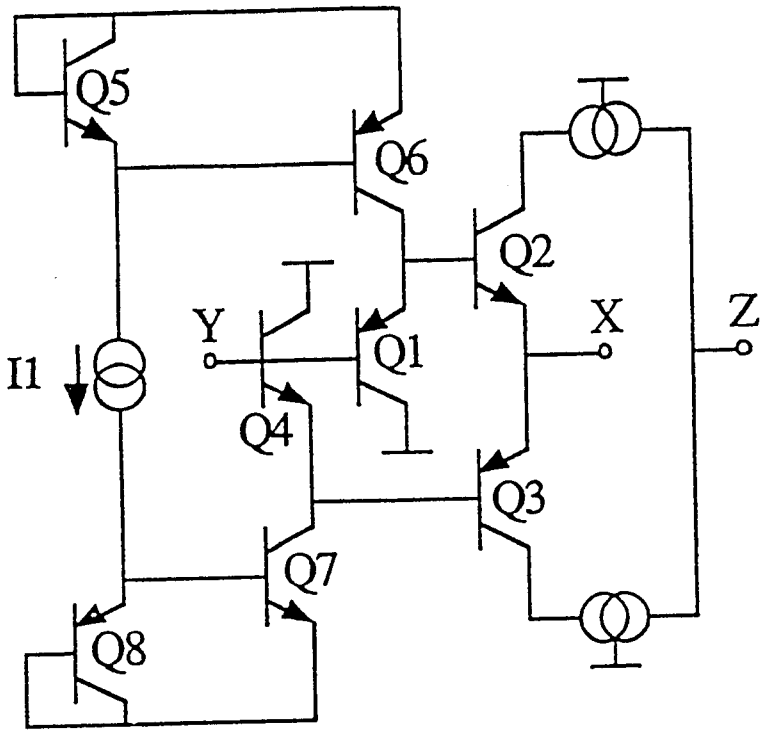


Figure 1(b)

2. (a) The circuit shown in *Figure 2* is a precision diode. Explain the operation of the circuit and sketch the corresponding waveforms at nodes Vx and Vo assuming an input sinusoidal signal. Derive an expression for the diode transfer function, and estimate the maximum input frequency, which would not result in a serious degradation in the quality of output signal. The slew-rate of the op-amp is 10 volts/μs.

[16 marks]

(b) A peak detector is required, capable of acquiring an input rectangular pulse of 2.5 V maximum amplitude and 900 ns minimum width. The output feeds a 10 bit ADC, which has a total conversion time of 350 μs. Sketch a suitable circuit to meet the above requirements and select suitable components to meet the specification. Assume the op-amp has a maximum output current limit of 10 mA. [5 marks]

(c) Finally, sketch a suitable circuit which achieves current-mode rectification without the use of a diode-based rectifier of the type shown in *Figure 2*. [4 marks]

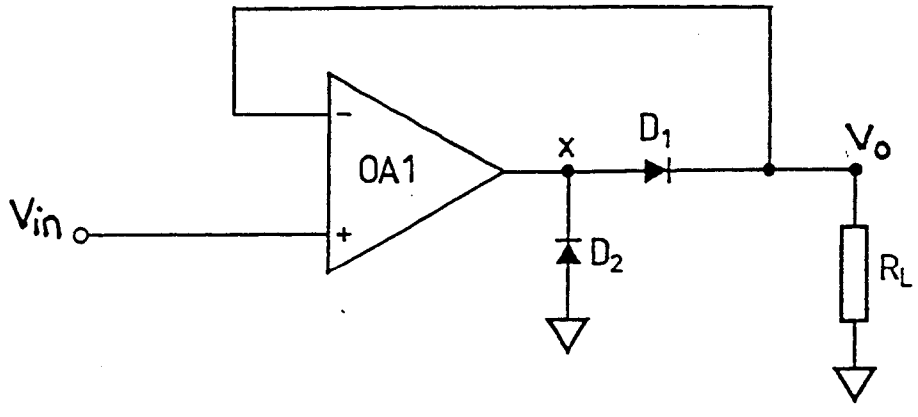


Figure 2

3. (a) The circuit in *Figure 3(a)* is a bootstrapped transconductance amplifier. Derive an expression for the output resistance of the amplifier and show that the minimum output resistance Rout(min) is 250 kΩ given that R3 = 10 kΩ and the resistors have a tolerance of ±1%. State any assumptions and matching conditions. [10 marks]

(b) High output resistance without the need for without resistor matching can be achieved with the circuit of *Figure 3(b)*. Explain the operation of the circuit and show how two of such circuits can realise a high CMRR differential amplifier, which also does not require precise resistor matching. [5 marks]

(c) In mixed-mode ASIC design, analogue design is constantly being optimised for digital CMOS technology and *Figure3(c)* shows an example referred to as a switched-current integrator. Derive an expression for the time constant of the integrator. Assume non-overlapping clocks and that all the switches are ideal. [10 marks]

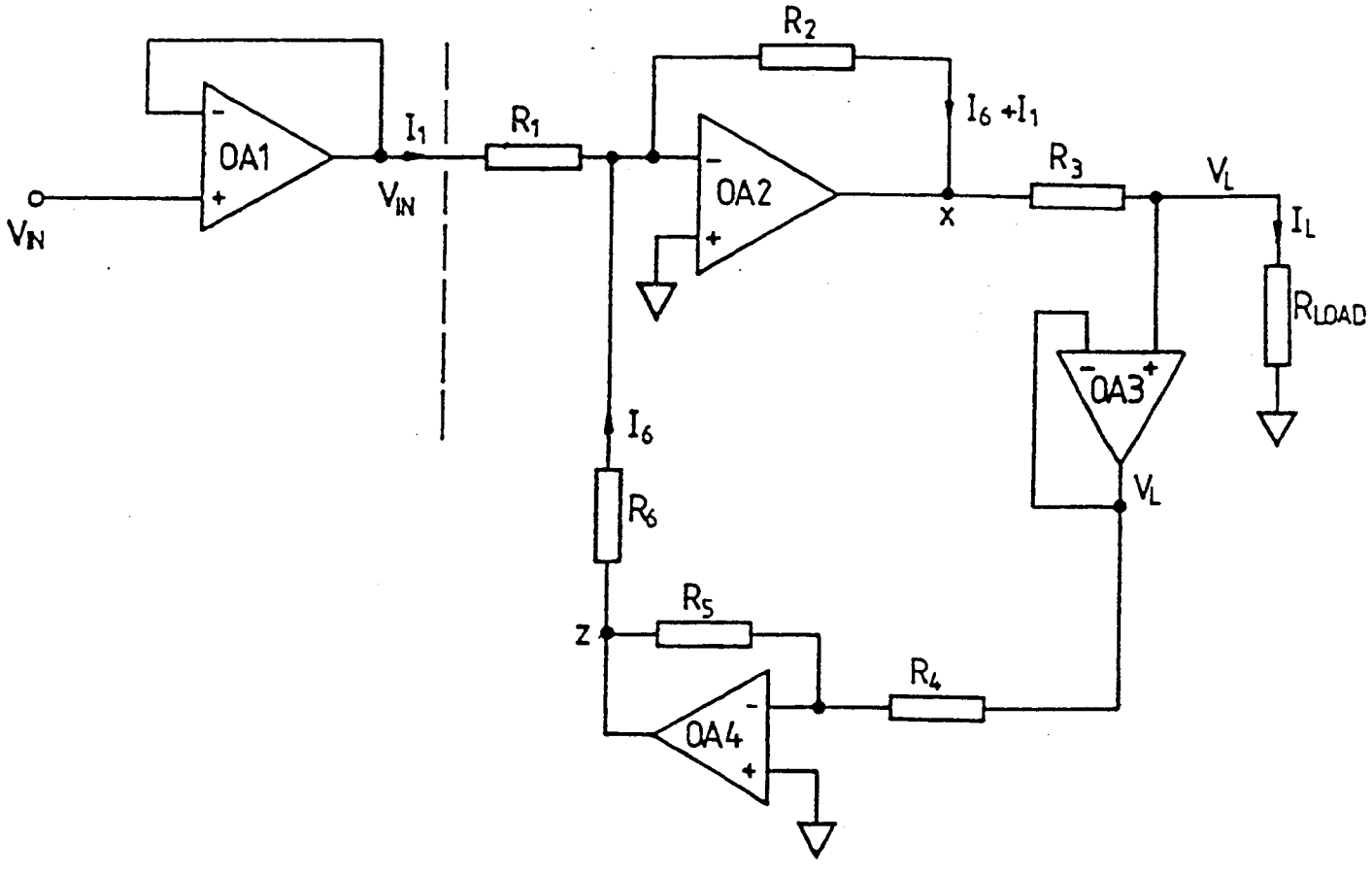


Figure 3 (a)

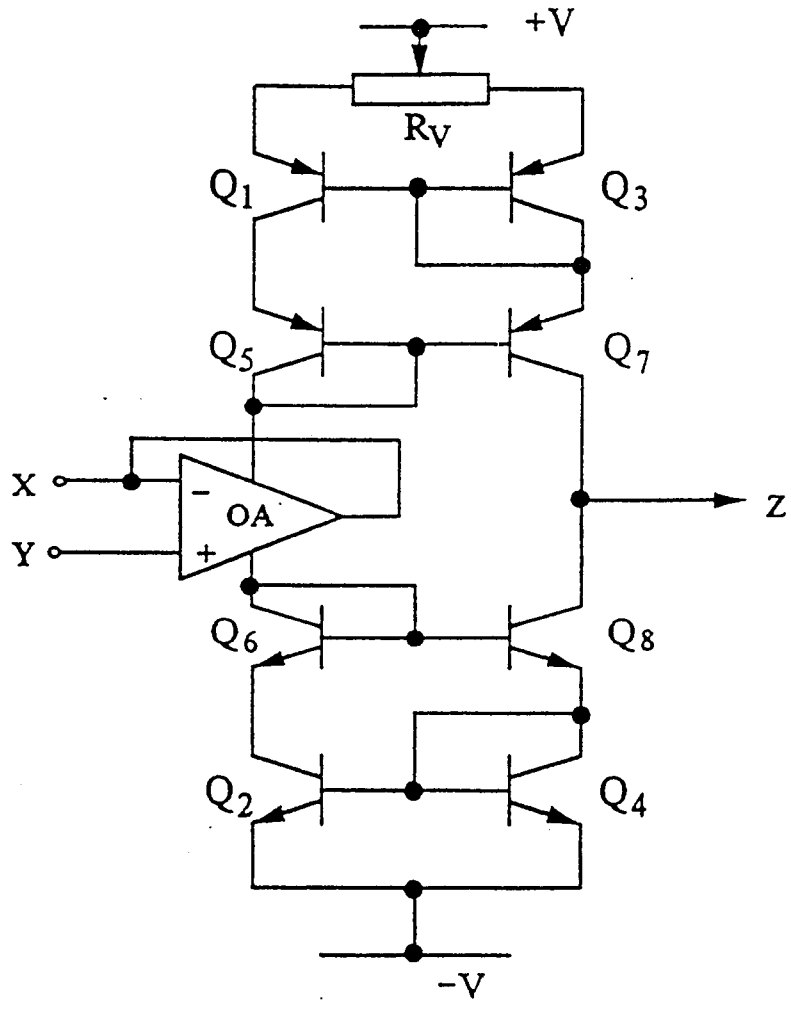


Figure 3(b)

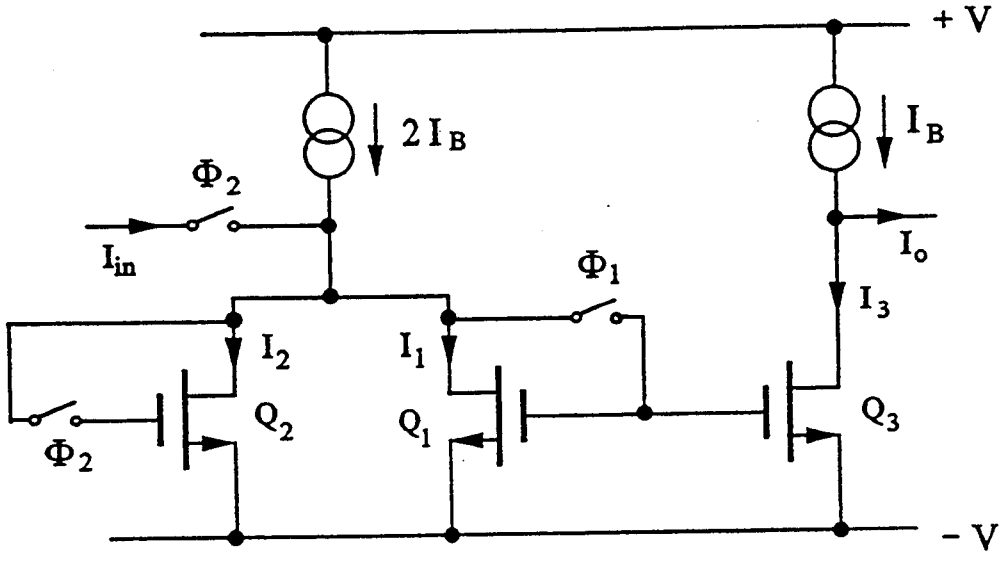


Figure 3(c)

4. (a) State the bipolar translinear principle (TLP) for a loop of p-n junctions. List five conditions which must be satisfied by the circuit in order for this principle to be valid. [5 marks]

(b) *Figure 4* shows two translinear circuits. For the circuit of *Figure 4a*, I_1 and I_3 are input currents while I_2 and I_4 are constant bias currents. Derive an expression for the output current I_{out} stating any assumptions that you make, and hence outline the function of this circuit. What is the minimum value which should be selected for I_2? Write down an expression for the output current when $I_1 = \left|\frac{dI_{in}}{dt}\right|$ and $I_3 = \left|\int I_{in}\, dt\right|$, given that $I_{in} = A \sin \omega t$. [10 marks]

For the circuit of *Figure 4b*, show that the output current :

$$I_{out} = I_1 - I_2 = \frac{I_3^2 - I_4^2}{\sqrt{\left(I_3^2 + I_4^2\right)}}$$

where I_3 and I_4 are input currents. Hence state the function of this circuit if $I_3 = I_A|\cos \omega t|$ and $I_4 = I_A|\sin \omega t|$. [10 marks]

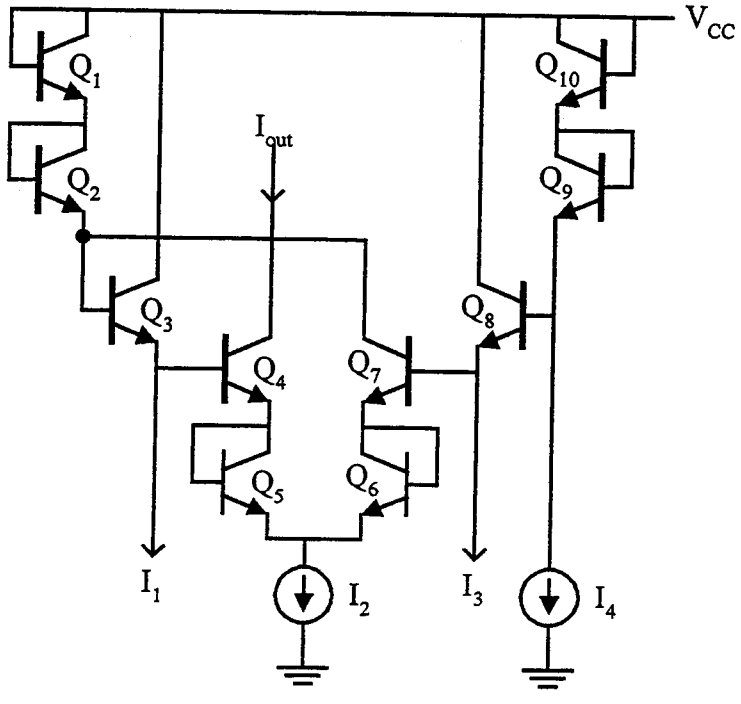


Figure 4a

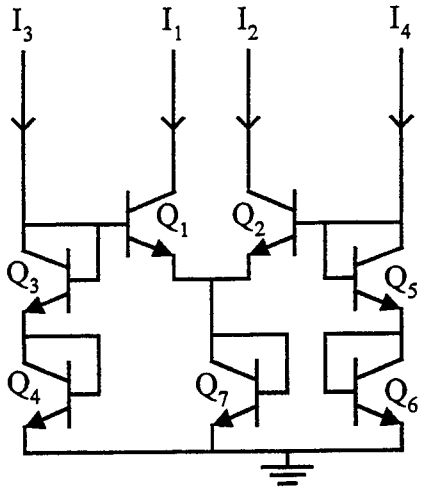


Figure 4b

5. The transfer function for a second order filter has been decomposed into the following state equations:

$$\dot{x}_1 = -\omega_0 x_2 + \omega_0 u_1$$
$$\dot{x}_2 = \omega_0 x_1 - \frac{\omega_0}{Q} x_2 + \omega_0 u_2$$
$$y = x_2$$

where y is the output, x_1 and x_2 are state variables, and u_1 and u_2 are inputs.

(a) Show that these state equations can be used to implement either a lowpass or a bandpass transfer function, and explain the role of the two inputs u_1 and u_2.

[7 marks]

(b) By the use of suitable exponential variable transforms, show that the linear state equations above can be transformed into non-linear log-domain design equations.

[8 marks]

(c) From these design equations, sketch a transistor level implementation of the final log-domain filter, and choose d.c. bias current values to give $\omega_0 = 2\pi(10 \times 10^6)$ rad s^{-1}. You may assume that all capacitors to be used are of value 10 pF. [10 marks]

6. (a) State the relationship which must be satisfied by two N-port networks, if these two networks are to be considered adjoint networks. By using this relationship, derive the adjoint network for (i) a resistor, (ii) a nullor, (iii) a unity gain voltage amplifier. Hence derive the current-mode equivalent of the Sallen-Key lowpass filter shown in *Figure 6a*. [13 marks]

(b) *Figure 6b* shows a transistor-level implementation of a unity gain current amplifier. Derive expressions for (i) the input offset voltage when $I_{in} = 0$, (ii) the small-signal input resistance for this circuit. Describe with the aid of a diagram how this circuit may be modified to simultaneously reduce the input offset voltage and small-signal input resistance. [12 marks]

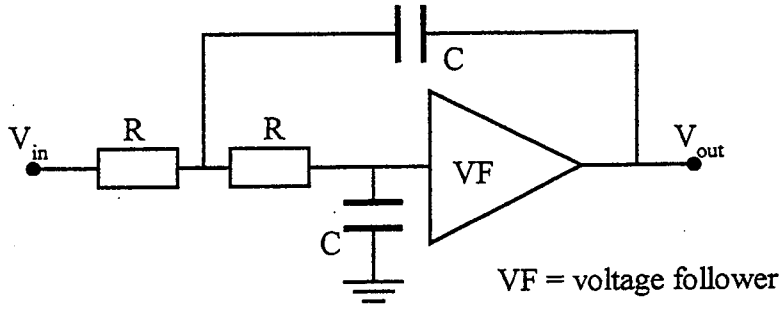


Figure 6a

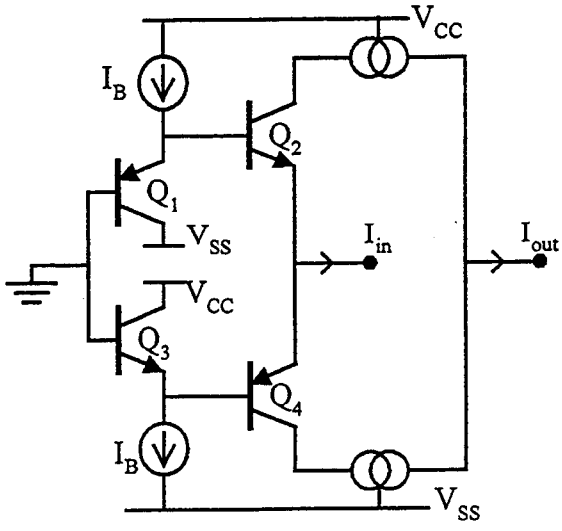
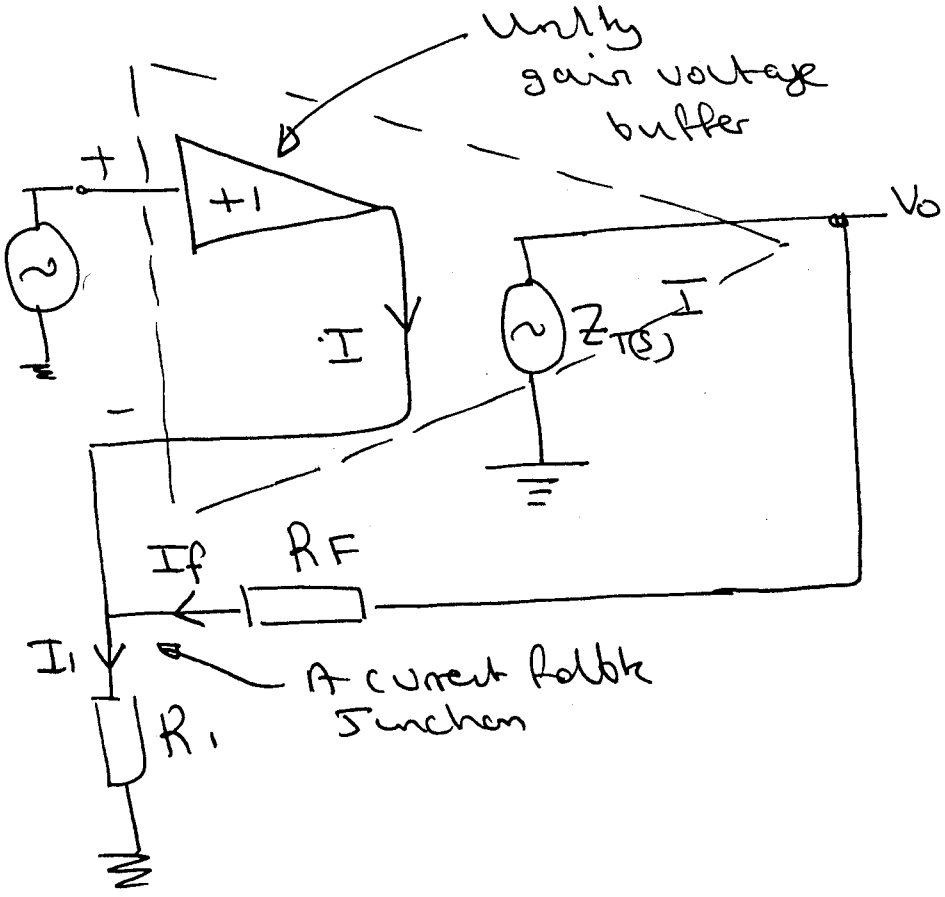


Figure 6b

(1) (1)

Current-feedback Amplifier

3/7/00
master
solutions



open-loop transresistance gain $Z_{T(S)}$

" voltage gain $A_{VS} = I Z_{T(S)}$

assume $Z_{T(S)} = Z_{TO}/(1 + jf/f_p)$

where f_p – dominant pole frequency of open-loop amplifier. From macromodel

3 principle equations

$$I_f = (V_o - V_S)/R_F \quad -(1)$$

$$I_1 = V_S/R_1 \quad -(2)$$

$$V_o = Z_{T(S)} I = Z_{T(S)}(I_1 - I_f) \quad -(3)$$

substituting (1) and (2) into (3) gives

5 —— $$(V_o/V_S) = (1 + R_F/R_1)\left(\frac{Z_{TS}}{R_F + Z_{TS}}\right) \quad -(4)$$

Assuming $Z_{T(S)} \gg R_F$

Then $V_o/V_S = (1 + R_F/R_1)$

1 cont

Since $Z_T(s)$ is the only frequency dependent term when gain is set almost independent of bandwidth

This is confirmed by substituting

$Z_T(s) = Z_{TO}/(1+jf/f_p)$ into (4)

$$\left(\frac{V_o}{V_s}\right) = \left(1+\frac{R_F}{R_1}\right)\left[\frac{Z_{TO}}{Z_{TO}+R_F}\right]\left[\frac{1}{\left(1+jf/f_p\left(\frac{Z_{TO}+R_F}{R_F}\right)\right)}\right]$$

Again assuming

$Z_{TO} \gg R_F$ then

$$(8)-\left(\frac{V_o}{V_s}\right)_{j\omega} = \left(1+\frac{R_F}{R_1}\right)\left(\frac{1}{1+jf/\frac{GB}{R_F}}\right) \quad -(8)$$

where $GB = f_p Z_{TO}$ = Gain bandwidth product.

Closed-loop bandwidth is thus

$f_{pc} = G \cdot B/R_F$

$R_F \rightarrow$ Bandwidth, $R_1 \rightarrow$ gain

—1—

Terminal relationship.

$V_x = V_y$, $I_z = \pm I_x$

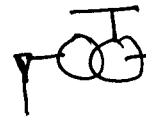
Versatile since device has both voltage mode and current-mode capability. —(4)

1 cont

Q_1, Q_2, Q_3, Q_4

So called 'diamond' voltage voltage.

Complimentary Class AB voltage followers.



supply current-sensing current-mirror

Sense X node current & output Z.

High output impedence.

Limit on dv_o/dt determined by push-pull action of Q_2 and Q_3. Maximum signal $I_{(max)}$ determined by power ratings of transistor or power supply current limit. 3/3

- Since $I_{(max)}$ is large then 2/2

$\left(dv/dt\right)_{max} = \left[I_{max}/C\right]$ ← provide also very large. ——— 5

Since by connection $V_{BE8} = V_{BE7}$

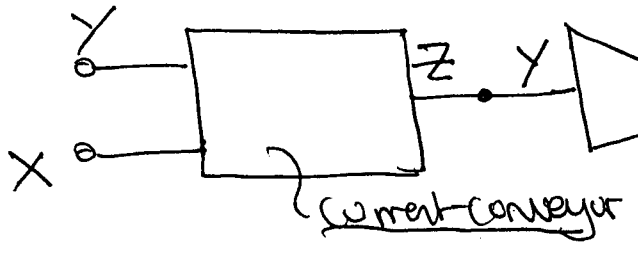
then $V_{B4} = V_{BE8}$

$V_X = \left(V_{BE4} + V_{BE3}\right) + V_Y$

V_{BE3} (P-device) $\Rightarrow$ $V_{BE4} = V_{BE}$ of P device

then $\left(V_X \cong V_Y\right)$ offset is reduced.

3

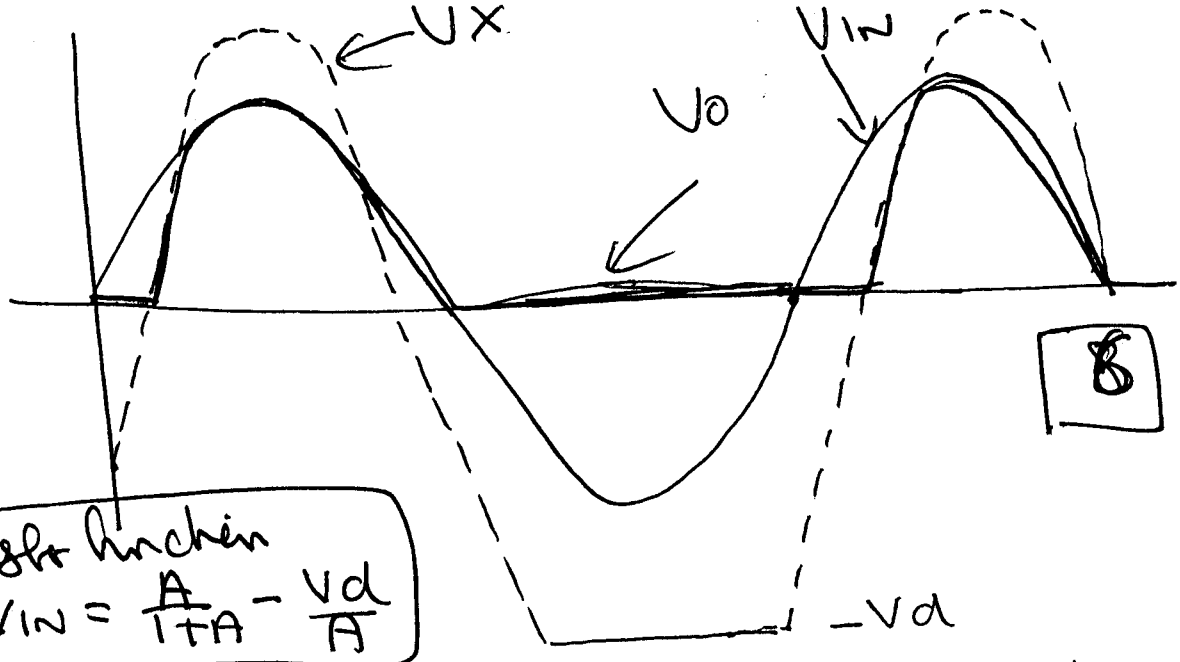


4 more.

25/25

2. Precision diode

OA1 and D1 half wave rectifier.
D1 conducts for positive input signal
For negative input OA1 output drops to −0.6 volts reducing recovery time. — 2
OA1 should be short circuit current protected.



3

8

Transfer function
$V_O/V_{IN} = \frac{A}{1+A} - \frac{V_d}{A}$

As can be seen the output is badly distorted when the diode is not conducting because the op-amp slewing holds the diode off even when $V_{IN} > 0$. This distortion becomes more significant as the input frequency rises.

Recovery or delay time is greater than

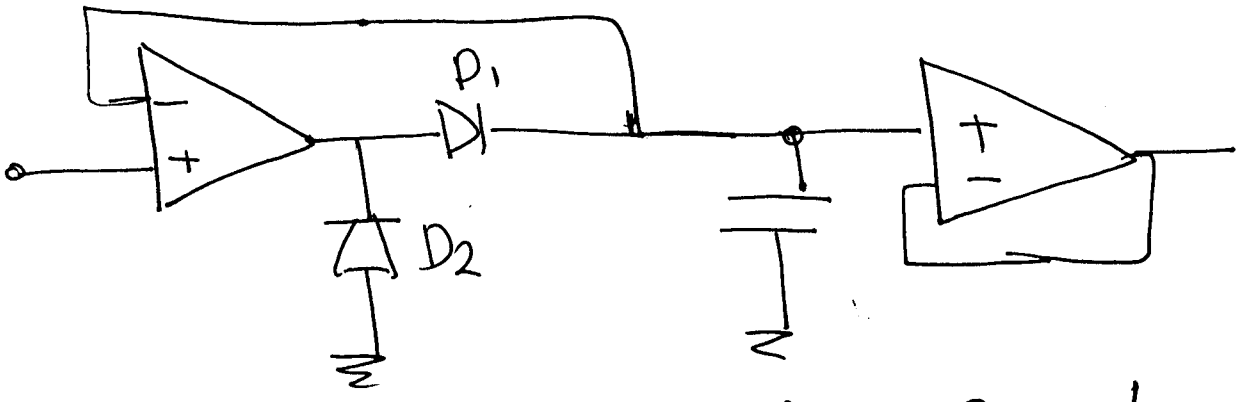
$$(1.2v/s \cdot R) = \underline{dt} = 0.12\mu s$$

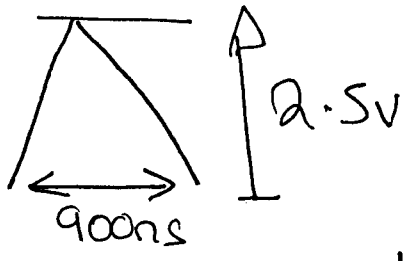
Since pulse width $\approx 0.12\mu s$
Period $\approx 0.24\mu s$ — 5

$$\underline{f = 4.16\ MHz}$$

2 cont

Peak detector





$\left.\frac{dv}{dt}\right|_{max} = \frac{2.5}{900ns} = 2.78 V/\mu s$

S.R of op amp

$\frac{I_{outmax}}{C} \leq 2.78 V/\mu s$

Let op-amp give $10mA \rightarrow I_{outmax}$ — 5

$C < \frac{10 \times 10^{-3}}{2.78 \times 10^{6}} = \frac{10}{2.78}\ nF = 3.5\ nF$

3.3 nF would do here

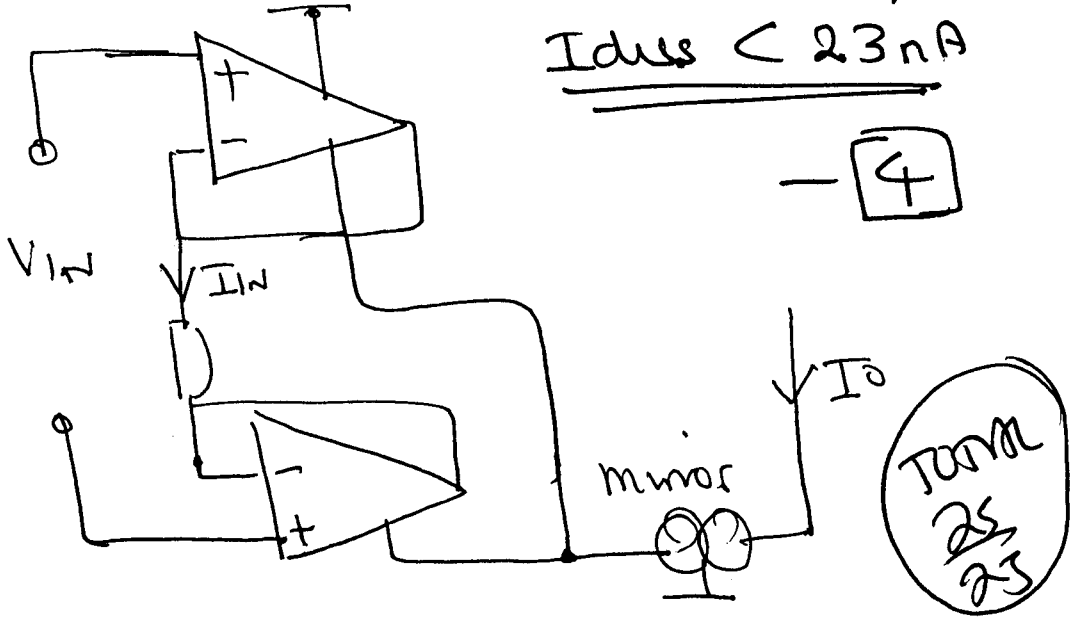
Last part

Current-mode readout

$\frac{I_{bias}}{C} < \frac{2.5}{1024} / 350 \times 10^{-6}$

$I_{bias} < 23 nA$

— 4



TOTAL 25/25

(3). Bootstrapped Current-source

With correct choice of R_5 the voltage across R_3 is made independent of V_L because V_X is of the form

$$V_X = kV_{IN} + V_L$$

$$I_3 = I_L = kV_{IN}/R_3$$

$$k = -R_2/R_1$$

iff $R_5/R_4 = R_6/R_2$

OR

$$I_L = -(R_2/R_1)V_{IN}/R_3 + [(R_2R_5)/(R_3R_4R_6) - 1/R_3]V_o$$

[5]

from which the output impedance is simply

$$-\delta V_o/\delta I_L = R_{out} \text{ and}$$

$$R_{out} = R_3R_4R_6/(R_4R_6 - R_2R_5)$$

$$= R_3/\left(1 - \frac{R_2R_5}{R_4R_6}\right)$$

Assume 1% resistors

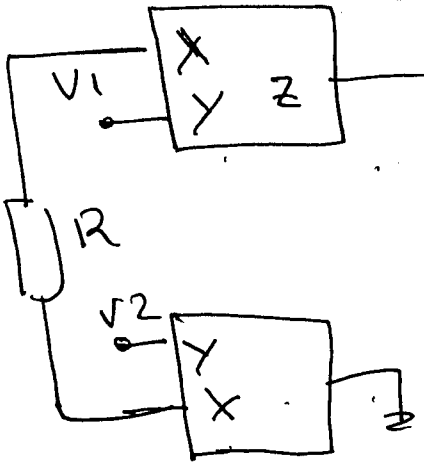
$$R_{out} = R_3/(1 - (1 + 0.04))$$

$$R_{out} \approx 25R_3 \approx \underline{\underline{250k\Omega}}.$$

[5]

3 cont

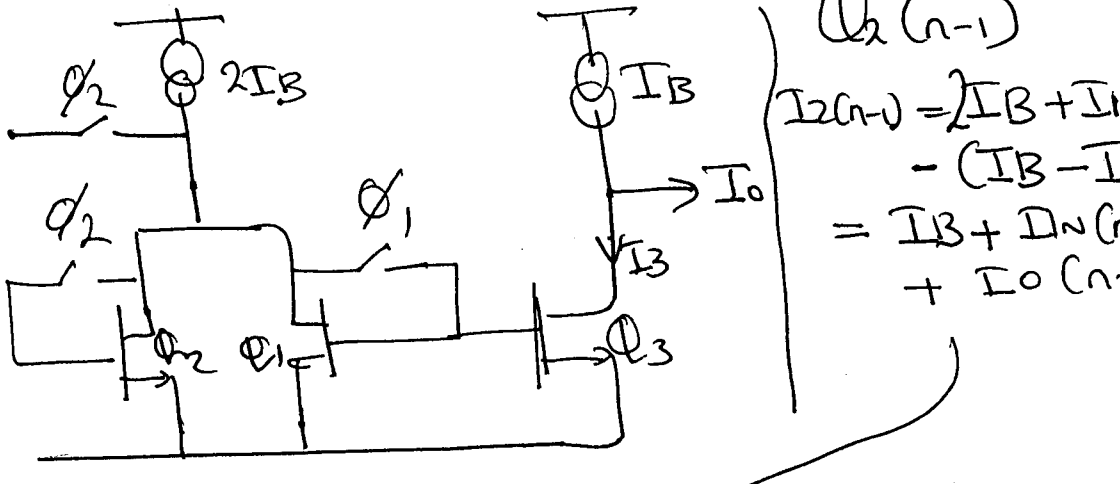
Supply current sensing circuit.
Current into X terminal drawn by power supplies and current mirror to high output impedence node Z. Current-mirrors are improved wilson type mirrors.
RV is essentially offset bias adjustment to ensure minimum offset at output due to imbalance in P and N mirrors.
Good voltage buffer between X and Y.
Current follower between X and Z.



$$I_o = \frac{(V_1 - V_2)}{R}$$

5

Basis of differential instrumentation amplifier.



$Q_2(n-1)$

$I_{2(n-1)} = 2I_B + I_{IN}(n-1) - (I_B - I_o(n-1))$
$= I_B + I_{IN}(n-1) + I_o(n-1)$

During $\phi_1(n)$

$I_1(n) = 2I_B - I_2(n-1) = I_B - I_{IN}(n-1) - I_o(n-1)$
$\Rightarrow I_o(n) = I_{IN}(n-1) + I_o(n-1)$

In z-domain

$$Lo(z)\left[1-z^{-1}\right) = Lin(z)\,z^{-1}$$

$$H(z) = \frac{Lo}{Lin}(z) = \left(\frac{z^{-1}}{1-z^{-1}}\right) = \frac{1}{z^{1}-1}$$

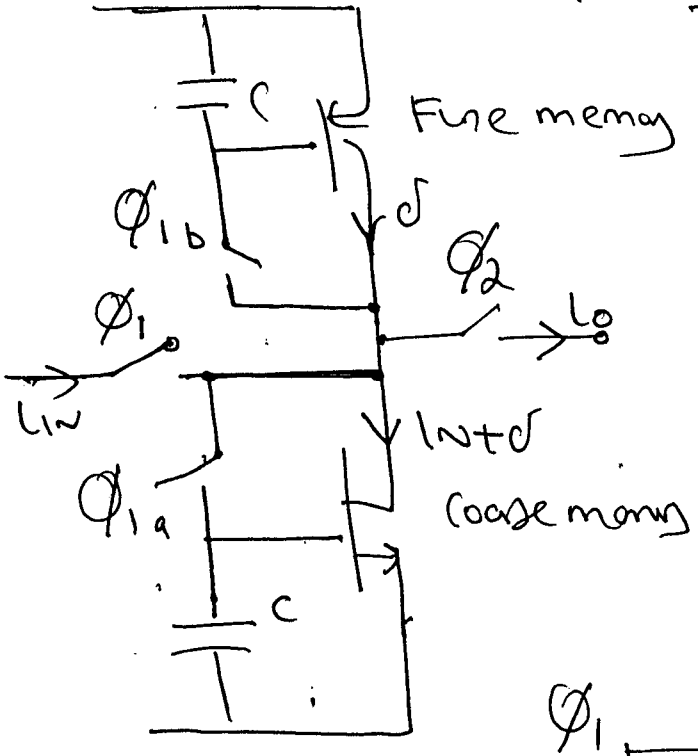
Since $e^{sT} = e^{j\omega T} \approx (1+j\omega T)$ for $\omega T \ll 1$

$\therefore H(z) = 1/j\omega T$ loss-less integrator

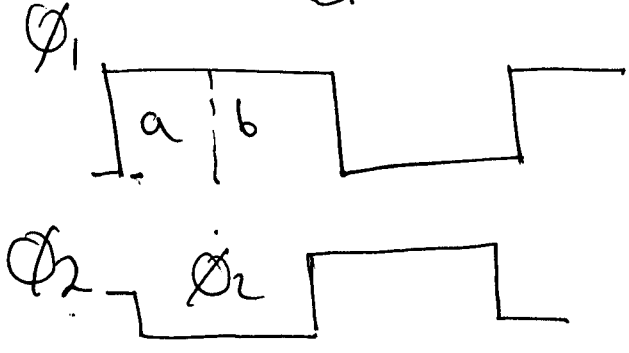
and so $\boxed{T=T}$ — 10 / 25/25

Ignore

Two step



Error in coase memory is stored by fine memory and then subtracted from stored output cancelling error.



4. Bipolar TLP:

$$cw\prod_{j=1}^{m}\frac{Ic_j}{A_j} = ccw\prod_{j=1}^{m}\frac{Ic_j}{A_j}$$

The product of the collector currents ÷ by the emitter areas for devices in a clockwise direction is equal to the product of the collector currents ÷ by the emitter areas for devices in a counter clockwise direction.

i) continuous loop of p-n junctions
ii) equal number of cw & ccw npn junctions
iii) equal number of cw & ccw pnp junctions
iv) all devices at same temperature (same V_T)
v) npn devices have same J_{sn}, similarly pnp devices all have same J_{sp}.
vi) all transistors must be forward biased (5)

figure 4a:

$$(I_2 - I_{out})^2 \cdot I_1 \cdot I_{out}^2 = (I_2 - I_{out})^2 \cdot I_3 \cdot I_4^2$$

Assuming transistors all have equal areas
β is high (ie base currents can be neglected)
V_A is high (ie Early voltage effects are neglected).

$$I_{out}^2 = I_4^2 I_3 / I_1$$

$$I_{out} = I_4 \cdot \sqrt{\frac{I_3}{I_1}}$$

The circuit calculates the square root of the quotient of the two inputs.

$I_{in} = A \sin \omega t$

$I_1 = |dI_{in}/dt| = A\omega \cos \omega t$

$I_3 = |\int I_{in}\, dt| = \frac{A}{\omega} \cos \omega t$

$\therefore \quad I_{out} = I_4 \sqrt{\frac{I_3}{I_1}} = I_4/\omega$

Output current is inversely proportional to the input frequency.

Let $I_A = (I_2 - I_{out})$ = bias current for Q_1, Q_2, Q_7, Q_6

I_A must remain positive to keep these devices forward biased, thus $I_2 > I_{out(max)}$ (10)

Figure 4b:

$$I_3^2 = I_1(I_1 + I_2) \qquad I_4^2 = I_2(I_1 + I_2)$$

$$I_3^2 = I_1^2 + I_1 I_2 \qquad I_4^2 = I_2^2 + I_1 I_2$$

$$I_3^2 - I_4^2 = I_1^2 - I_2^2 = (I_1 - I_2)(I_1 + I_2)$$

$$I_3^2 + I_4^2 = I_1^2 + 2I_1 I_2 + I_2^2 = (I_1 + I_2)^2$$

$$(I_1 - I_2) = \frac{(I_3^2 - I_4^2)}{(I_1 + I_2)} = \frac{I_3^2 - I_4^2}{(I_3^2 + I_4^2)^{1/2}}$$

$I_3 = |A|\cos\omega t|$ $\quad I_4 = |A|\sin\omega t|$

$$I_1 - I_2 = \frac{|A^2\cos^2\omega t - |A^2\sin^2\omega t}{(|A^2\cos^2\omega t + |A^2\sin^2\omega t)^{1/2}}$$

$$= \frac{|A^2(\cos^2\omega t - \sin^2\omega t)}{|A}$$

$$= |A(\cos^2\omega t - \sin^2\omega t)$$

$$= |A(\cos^2\omega t - (1-\cos^2\omega t))$$
$$= |A(2\cos^2\omega t - 1)$$
$$= |A(1+\cos 2\omega t - 1)$$
$$= |A\cos 2\omega t$$

The circuit is a frequency doubler (10)

5. $\dot{x}_1 = -\omega_0 x_2 + \omega_0 u_1$

$\dot{x}_2 = \omega_0 x_1 - \frac{\omega_0}{Q} x_2 + \omega_0 u_2$

$y = x_2$

$\ddot{x}_2 = \omega_0 \dot{x}_1 - \frac{\omega_0}{Q} \dot{x}_2 + \omega_0 \dot{u}_2$

$\ddot{x}_2 = \omega_0(-\omega_0 x_2 + \omega_0 u_1) - \frac{\omega_0}{Q} \dot{x}_2 + \omega_0 \dot{u}_2$

$\ddot{x}_2 + \omega_0^2 x_2 + \frac{\omega_0}{Q} \dot{x}_2 = \omega_0^2 u_1 + \omega_0 \dot{u}_2$

Taking Laplace Transform:

$$X_2(s)\left[s^2 + s\omega_0/Q + \omega_0^2\right] = \omega_0^2 U_1(s) + \omega_0 \cdot s \cdot U_2(s)$$

$$Y(s) = X_2(s)$$

$$\therefore \frac{y(s)}{u_1(s)} = \frac{\omega_0^2}{s^2 + s\omega_0/Q + \omega_0^2} \quad \text{if } u_2 = \emptyset$$

LOWPASS

$$\frac{y(s)}{u_2(s)} = \frac{s\omega_0}{s^2 + s\omega_0/Q + \omega_0^2} \quad \text{if } u_1 = \emptyset$$

BANDPASS.

u_1 = input for lowpass t.f

u_2 = input for bandpass t.f.

The input which is not being 'utilised' will generally be a dc current to maintain dc bias conditions.

(7)

Let $X_1 = I_0 e^{V_1/V_T}$ $\quad X_2 = I_0 e^{V_2/V_T}$

$$\dot{X}_1 = \frac{X_1}{V_T}\dot{V}_1 \qquad \dot{X}_2 = \frac{X_2}{V_T}\cdot\dot{V}_2$$

$$U_1 = I_S e^{V_{u1}/V_T} \qquad U_2 = I_S e^{V_{u2}/V_T}$$

$$\Rightarrow \frac{X_1}{V_T}\dot{V}_1 = -\omega_0 X_2 + \omega_0 U_1$$

$$\frac{X_2}{V_T}\dot{V}_2 = \omega_0 X_1 - \frac{\omega_0}{\varphi} X_2 + \omega_0 U_2$$

$$\Rightarrow C\dot{V}_1 = -C\omega_0 V_T \frac{X_2}{X_1} + C V_T \omega_0 \frac{U_1}{X_1}$$

$$C\dot{V}_2 = C V_T \omega_0 \frac{X_1}{X_2} - \frac{C V_T \omega_0}{\varphi} + C V_T \omega_0 \frac{U_2}{X_2}$$

Let $I_0 = C V_T \omega_0$

$$\Rightarrow C\dot{V}_1 = -I_0 \cdot \exp\frac{(V_2 - V_1)}{V_T} + I_S \exp\frac{(V_{u1} - V_1)}{V_T}$$

$$C\dot{V}_2 = I_0 \exp\frac{(V_1 - V_2)}{V_T} - \frac{I_0}{\varphi} + I_S \exp\frac{(V_{u2} - V_2)}{V_T}$$

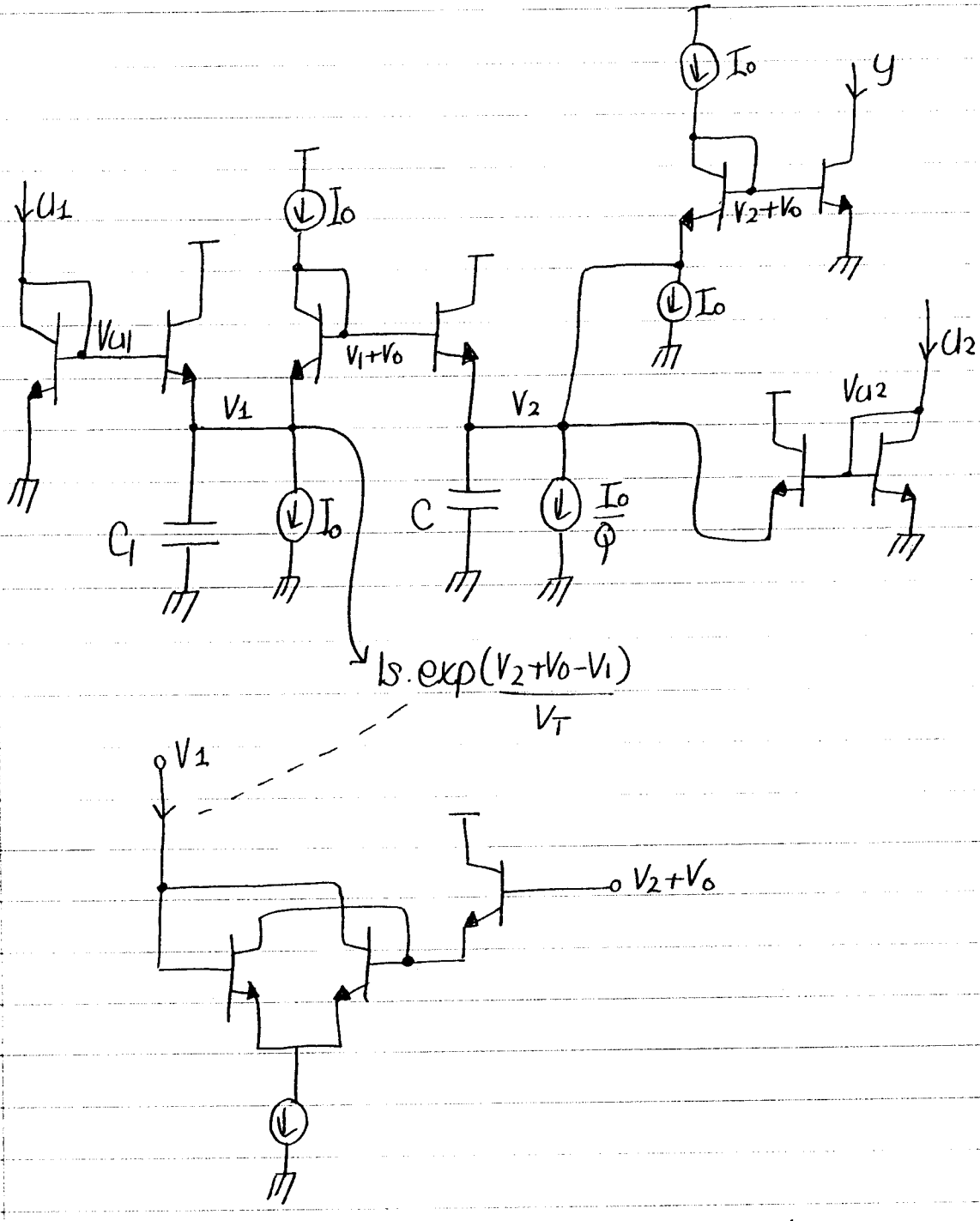
Let $I_0 = I_S \exp(V_0/V_T)$

$$\Rightarrow C\dot{V}_1 = -I_S \cdot \exp(V_2 + V_0 - V_1)/V_T + I_S \cdot \exp(V_{u1} - V_1)/V_T$$

$$C\dot{V}_2 = I_S \cdot \exp(V_1 + V_0 - V_2)/V_T - \frac{I_0}{\varphi} + I_S \exp(V_{u2} - V_2)/V_T$$

$$y = X_2 = I_o e^{V_2/V_T} = I_s \exp(V_2+V_o)/V_T$$

CIRCUIT DIAGRAMS :



For B.P operation, we can remove u_2 stage.
For B.P operation, u_1 stage must be present for correct dc biasing. (8)

$I_o = C\omega_o V_T \quad \therefore \omega_o = \frac{I_o}{CV_T}$

$I_o = 10p \cdot 2\pi (10 \times 10^6) 25 \times 10^{-3}$ (2)

$= 15.7\ \mu A.$

6 (a) Two N-port networks (A & B) must satisfy the following relationship in order to be adjoint networks:

$$\sum_{n=1}^{N} \{ V_{An} I_{Bn} - I_{An} V_{Bn} \} = \emptyset$$

where V_{An} = voltage at n^{th} port of network A, etc. (2)

(i) Resistor

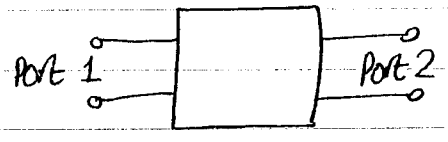
$V_A = I_A \cdot R_A$, one port

$$V_A \cdot I_B - I_A V_B = 0$$

$$\frac{V_A}{I_A} = \frac{V_B}{I_B} \quad \therefore \quad \frac{V_B}{I_B} = R_A$$

The adjoint network is a resistor of the same value. (2)

(ii) Nullor



$V_A = [V_{A1} \; V_{A2}] = [0 \; X]$

$I_A = [I_{A1} \; I_{A2}] = [0 \; X]$

$$V_{A1} I_{B1} - I_{A1} V_{B1} + V_{A2} I_{B2} - I_{A2} V_{B2} = \emptyset$$

$$0 \cdot I_{B1} - 0 \cdot V_{B1} + X \cdot I_{B2} - X V_{B2} = \emptyset$$

($0 \cdot I_{B1}$: 0 → X; $0 \cdot V_{B1}$: 0 → X; $X \cdot I_{B2}$: X → $\emptyset$; $X V_{B2}$: X → $\emptyset$)

[X = ANY VALUE!]

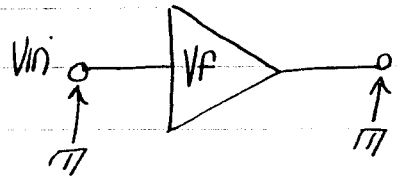
Thus $V_B = [V_{B1} \; V_{B2}] = [X \; 0]$

$I_B = [I_{B1} \; I_{B2}] = [X \; 0]$

(2)

Nullor, but with input & output ports interchanged.

(iii)



$V_A = [V_{A1}\ V_{A2}] = [V_{in}\ V_{in}]$

$I_A = [I_{A1}\ I_{A2}] = [0\ \ X]$

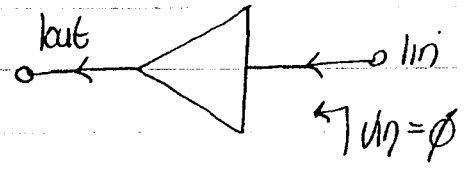
$$V_{A1} \cdot I_{B1} - I_{A1} \cdot V_{B1} + V_{A2} \cdot I_{B2} - I_{A2} V_{B2} = \emptyset$$

$$V_{in} \cdot I_{B1} - \underbrace{0 \cdot V_{B1}}_{X} + V_{in} \cdot I_{B2} - \underbrace{X \cdot V_{B2}}_{\emptyset} = \emptyset$$

$$V_{in} \cdot I_{B1} + V_{in} \cdot I_{B2} = \emptyset \qquad I_{B1} = -I_{B2}$$

$\therefore$ $V_B = [V_{B1}\ V_{B2}] = [X\ \ 0]$

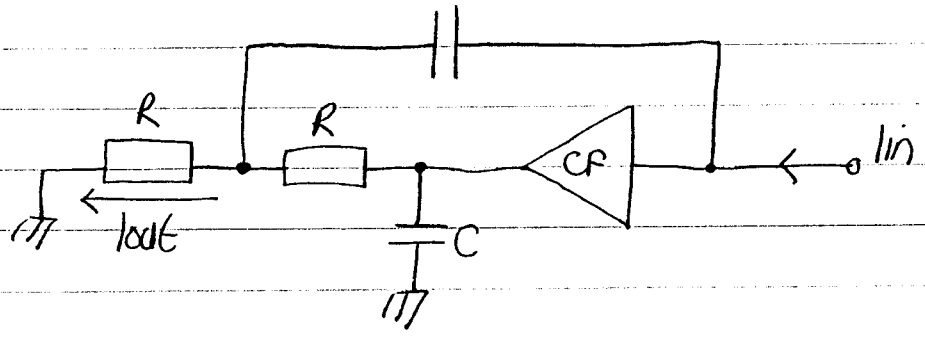
$I_B = [I_{B1}\ I_{B2}] = [I_{in} \cdot I_{in}]$



(2)

Unity gain current amp with input = port 2 & output = port 1.

Adjoint of Sallen-key filter:



(5)

(b). $V_{in} = V_{be1} - V_{be2}$

(i) In the absence of an input signal I_{in}, $I_{c2} \simeq I_{c4}$.
Also $I_{c1} \simeq I_{c3}$

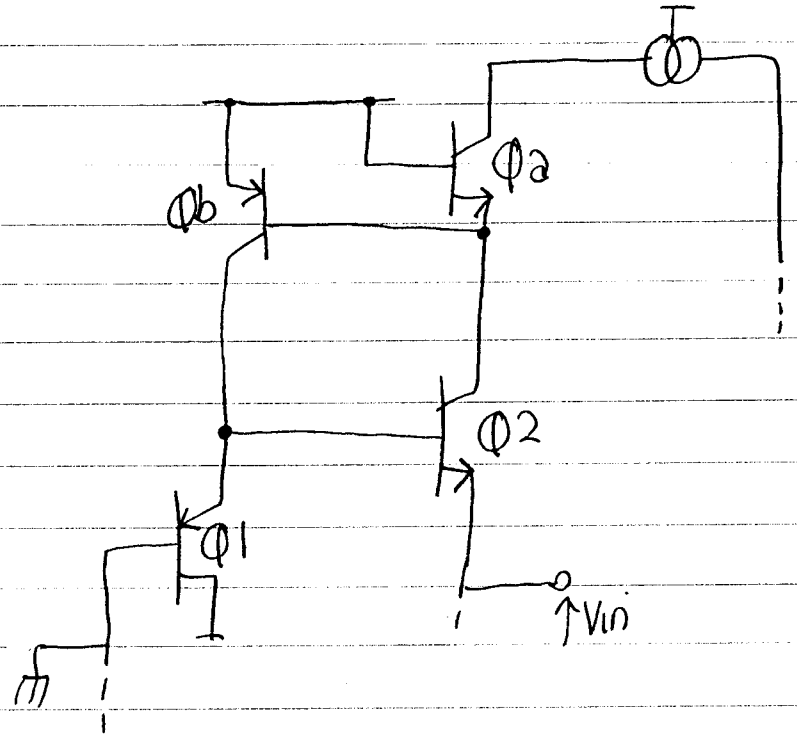
Thus $V_{be1} + V_{be3} = V_{be2} + V_{be4}$
Q_1 & Q_4 are matched, Q_2 & Q_3 are matched,
$\therefore I_{c1} = I_{c2} = I_{c3} = I_{c4} = I_B$.

$$V_{in} = V_T \ln\left(\frac{I_B}{I_{sp}}\right) - V_T \ln\left(\frac{I_B}{I_{sn}}\right) = V_T \ln\left(\frac{I_{sn}}{I_{sp}}\right)$$

'Dc' offset which will vary with temp.

(ii) Small signal input resistance, $r_{in} = r_{e2} // r_{e3}$
$$= \frac{V_T}{I_{c2}} \Big\| \frac{V_T}{I_{c3}}$$

To reduce V_{in} & r_{in} simultaneously:



$V_{in} = V_{be1} - V_{be2}$

$V_{be2} = V_T \ln(I_{c2}/I_{sn})$

$V_{be(Q2)} = V_T \ln(I_{c2}/I_{sn})$ [Matched to Q2]

$$I_{c(Qb)} = I_{sp} \cdot \exp\left(\frac{V_{be(Q2)}}{V_T}\right) = I_{sp} \cdot \exp[\ln I_{c2}/I_{sn}]$$

$$= \frac{I_{sp} \cdot I_{c2}}{I_{sn}}$$

$I_{c1} = I_{c(Qb)}$ $\therefore V_{be1} = V_T \ln(I_{c(Qb)}/I_{sp})$

$= V_T \ln(I_{c2}/I_{sn})$

i.e $V_{be1} = V_{be2}$

Thus V_{in} & r_{in} are reduced to zero. (12)