Master copy - June 07

E3.14
AO7

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2007

MSc and EEE PART III/IV: MEng, BEng.and ACGI

POWER ELECTRONICS AND MACHINES

Monday, 23 April 10:00 am

Time allowed: 3:00 hours

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks.

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible First Marker(s) : T.C. Green, P.D. Mitcheson
Second Marker(s) : B. Chaudhuri, B. Chaudhuri

Special instructions for invigilators

None

Special instructions for students

None

1.

a) Explain using the aid of diagrams how a double-diffused MOSFET structure is more suited to power processing applications than the typical lateral structure of a signal MOSFET. [5]

b)

i) Assuming an abrupt junction between the ***p***-body region and the ***n***$^-$-drift region in the power MOSFET, as shown in Figure 1, what is the minimum length required of the drift region to block 200 V? You can assume that the vast majority of the voltage is blocked in the ***n***$^-$-drift region and that the doping concentration in each region is constant. The maximum field strength in silicon before avalanche breakdown is 10 MV/m, the permittivity of free space is 8.85×10^{-12} F/m and the relative permittivity of silicon is 11.7. [3]

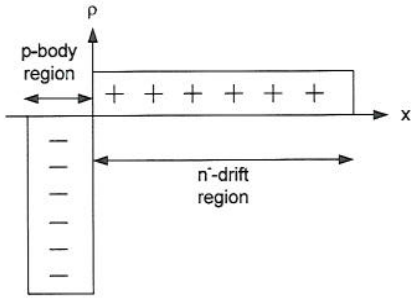


Figure 1 Charge distribution in an abrupt *p*-*n*$^-$ junction

ii) What doping density is required in the ***n***$^-$-region to achieve the 200 V blocking capability over this length? The charge on an electron is 1.6×10^{-19} C. [2]

c) The resistivity of n-type silicon is given by:

$$\rho = \frac{1}{N_D e \mu_e}$$

Where N_D is the concentration of donor atoms, e is the charge on the electron (1.6×10^{-19} C) and μ_e is the electron mobility which is $0.135 m^2/Vs$.

Calculate the resistivity of the ***n***$^-$-drift region and the required cross sectional area of the drift region such that the conduction loss in the device does not exceed 1 W/mm^2 at a rated current of 10 A. Assume that the power loss in the ***n***$^-$-drift region dominates the conduction loss. [5]

d) Explain how high-level injection in a simple ***p***$^+$***n*** diode causes additional conduction loss at a particular current beyond that predicted by the Shockley equation. Explain how a ***pin*** diode structure avoids this additional loss. [5]

2. Consider the circuit of Figure 2 which is an IGBT switching an inductive load:

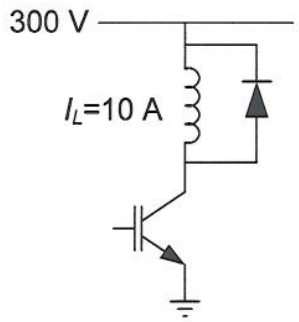


Figure 2 IGBT switching an inductive load

a) Explain how the inductively switched load gives rise to significant switching loss in the transistor at turn off. Draw a diagram of a turn off snubber applied to this circuit and explain how the snubber can reduce the turn off loss. [5]

b) Given that the current fall time and voltage rise are both 0.5 μs, calculate the turn-off switching energy loss per cycle in the snubberless IGBT with an inductor current of 10 A and a supply voltage of 300 V. [3]

c) For a room temperature of 21 °C and allowing a junction temperature of the IGBT of 100 °C, what should be the maximum thermal resistance between the heat sink and the air if the snubberless device is to be operated at a switching frequency of 100 kHz? What is the temperature of the heat sink under these conditions? Assume that the power losses are dominated by turn-off loss, that the thermal resistance between the junction and case is 0.25 °C/W and that the thermal resistance between the case and the heat sink is 0.12 °C/W. [3]

d) Design a snubber such that the turn off loss in the IGBT is reduced by a factor of 20. The minimum duty cycle of the IGBT will be 50 % and the current falls linearly in a time of 0.5 μs. [7]

e) Calculate whether the circuit with the snubber is more or less efficient than the circuit without the snubber. [2]

3.

a) Explain why the isolated Flyback converter is sometimes constructed with two MOSFETS rather than one. Comment on the voltage rating required of the MOSFETS in each case. [4]

b) Explain why the power factor of a simple diode rectifier is expected to be significantly less than unity. Comment on the consequences of this? [4]

c) Describe how the amplitude and frequency of the fundamental output of an inverter can be controlled. [4]

d) Describe the relative merits of on-line and off-line forms of uninterruptible power supply. [4]

e) Explain what is meant by four-quadrant operation of an electrical drive system and give examples of when operation in each quadrant is required. [4]

4.

(a) Explain why quasi-resonant circuits are sometimes used in switch-mode power supplies. [4]

(b) Figure 4.1 shows a zero-current switched quasi-resonant circuit and figure 4.2 shows the four periods of operation defined by the capacitor voltage and inductor current of the resonant circuit. Describe the circuit action in each of the four periods. [6]

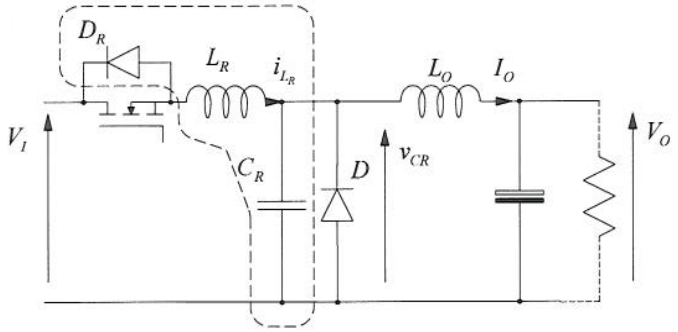


Figure 4.1 *A zero-current switched quasi-resonant circuit*

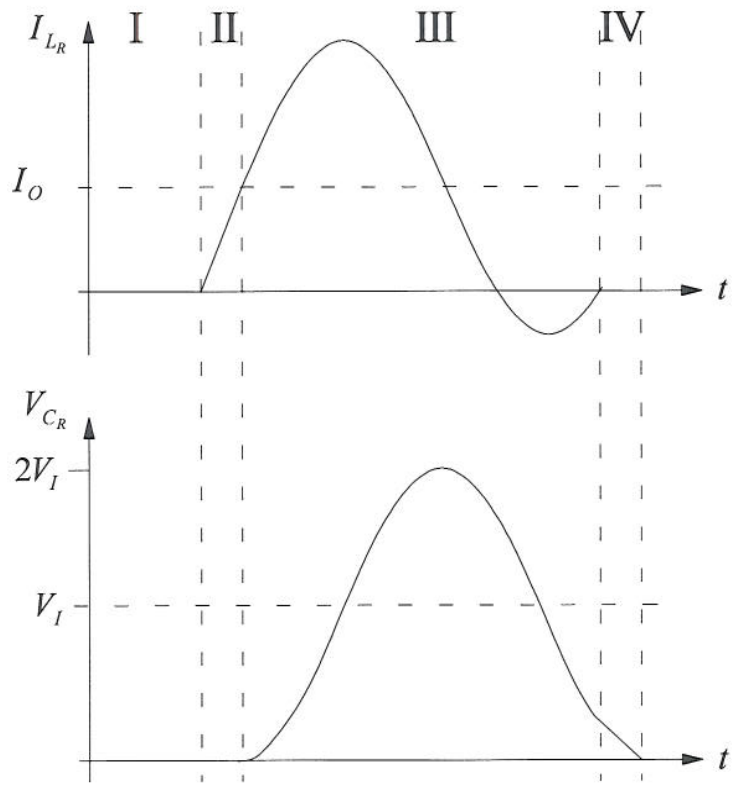


Figure 4.2 *The four periods of operations of a zero-current switched quasi-resonant circuit*

(c) A circuit is to be designed for $V_I = 24$ V, $V_o = 10$ V and $I_o = 1$ A. It has already been decided that the resonant frequency of the C_R and L_R combination will be 250 kHz. Find the overall period with which the circuit will need to be operated. [3]

You may use the result that during period III the circuit is governed by the equations:

$$i_{L_R} = I_o + \frac{V_i}{\omega L_R} \sin(\omega t)$$

$$v_{C_R} = V_i \left(1 - \cos(\omega t)\right)$$

(d) Mark on a sketch of the graph of i_{LR} the limits of the period during which the transistor can be switched off under zero current conditions. [2]

(e) It is desired to have at least a 200 ns period in which to turn off-the transistor. State the angle that this time represents with respect to the resonant cycle of C_R and L_R. Choose a value of L_R, and hence C_R, to achieve the desired turn-off window. [5]

5.

(a) Compare and contrast the Cúk and buck-boost switch mode power supplies, SMPS. [5]

(b) Derive the relationship between input and output voltage for the Cúk SMPS. [5]

(c) A power supply is to be designed that is subject to size constraints and voltage ripple tolerance. The outline specification is for conversion of +15V to -5V at an output current of 2A.

(i) Calculate the current flowing in the inductor of the buck-boost SMPS and both inductors of the Cúk SMPS. [5]

(ii) Given the constraint that the LI^2 of the inductors is limited to 10^{-3} HA^2 for the buck-boost and $0.5x10^{-3}$ for each inductor in the Cúk, calculate the value of the inductors. Calculate the peak-to-peak ripple current flowing in the input of each SMPS and the peak-to-peak output voltage ripple if the output capacitor has an effective series resistance of 40mΩ and the switching frequency is 40 kHz. [5]

6.

(a) Describe the operation of a brushless dc motor. Provide block diagrams of the systems and a sketch of the power converter circuit. [7]

(b) Compare the power converter circuit to the power converter circuit required for a traditional (brushed) dc motor to be operated in forward and reverse rotation with braking and accelerating torque. [4]

(c) Justify the shape of the torque-speed diagram in figure 6 with respect to a dc machine. Calculate the principal points on the diagram for a system with the following properties:

DC input voltage:	100 V
Armature resistance:	0.5 Ω
Field flux at maximum field current:	18 mWb
Armature constant:	12.5 $V.s.rad^{-1}.Wb^{-1}$ (or $N.m.A^{-1}.Wb^{-1}$)
Rated armature current:	8 A

[5]

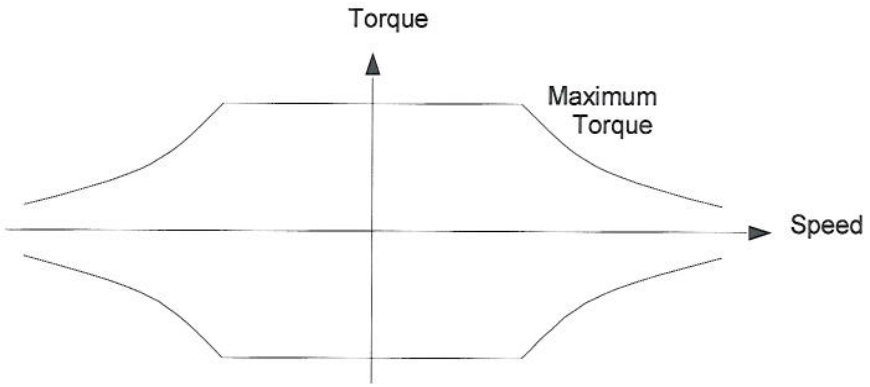


Figure 6 *A typical torque speed diagram of an electrical drive system*

(d) Summarise the relative merits of brushed and brushless dc drive system. [4]

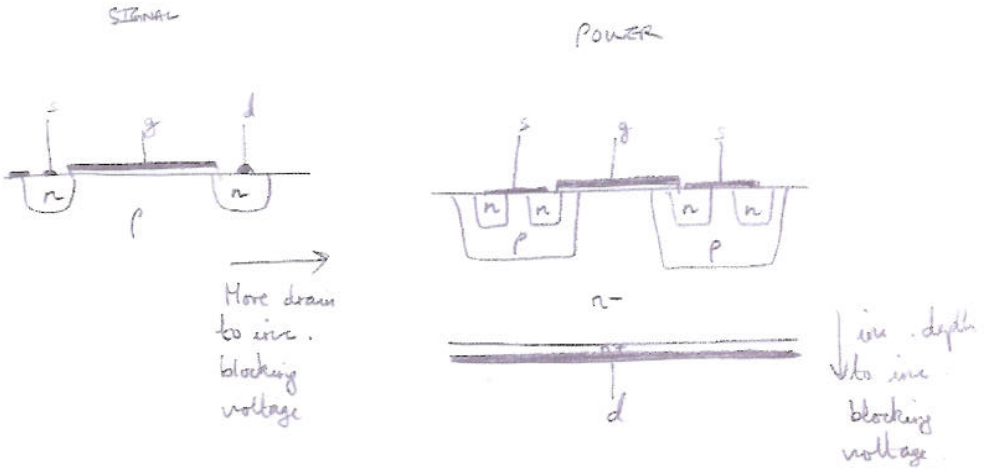
Power Electronics & Machines E3.14/A07

Model Answers - 2007 - Master.

1.

i) Explain using the aid of diagrams how a double-diffused MOSFET structure is more suited to power processing applications than the typical lateral signal MOSFET structure.

[5]



Essentially bookwork:

A power MOSFET must be able to carry large current and block high voltage. The double diffused structure used in the power device allows a long depletion layer to form (necessary for high voltage blocking) vertically in the wafer and thus the high voltage requirement does not lead to increased die area usage. If a lateral structure were used the drain would have to be a long way from the source to support a high blocking voltage and so die usage is inefficient. In addition, in the double diffused structure the n- region shields the gate oxide from having to support the entire blocking voltage.

ii)

a) Assuming an abrupt junction between the ***p***-body region and the ***n***$^-$-drift region in the power MOSFET, as shown in Figure 1, what is the minimum length required of the drift region to block 200 V? You can assume that the vast majority of the voltage is blocked in the ***n***$^-$-drift region and that the doping concentration in each region is constant. The maximum field strength in silicon before avalanche breakdown is 10 MV/m, the permittivity of free space is 8.85×10^{-12} F/m and the relative permittivity of silicon is 11.7.

[3]

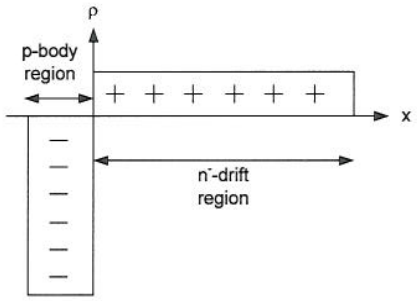
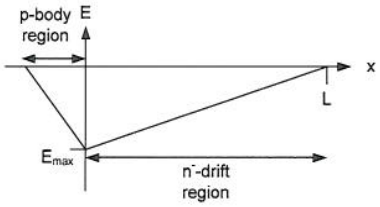


Figure 1 Charge distribution in an abrupt p-n^- junction

New calculations for students – they know the formulae but have not seen examples:

The electric field distribution is as shown below:



If we assume (as we are requested to) that almost all the blocking voltage appears across the n- region:

$$V_{block} = -\int E dx$$

$$= \frac{1}{2} E_{\max} L$$

Thus:

$$L_{drift} = \frac{400}{10 \times 10^6} = 40 \mu m$$

b) What is the doping density in the n^--region to achieve the 200 V blocking capability over this length? The charge on the electron is 1.5×10^{-19} C.

[2]

Poisson's equation tells us that:

$$E = -\frac{1}{\varepsilon_0 \varepsilon_r} \int \rho dx$$

Where ρ is charge density.

Thus:

$$\rho = \varepsilon_0 \varepsilon_r \frac{dE}{dx}$$

Therefore:

$$\rho = 8.85 \times 10^{-12} \times 11.7 \times \frac{10 \times 10^6}{40 \times 10^{-6}} = 25.88 C/m^3$$

And thus the doping density of donors is given by:

$N_D = 25.88/1.6 \times 10^{-19} = 1.6 \times 10^{20}/m^3 = 1.6 \times 10^{14}/cm^3$

iii) The resistivity of n-type silicon is given by:

$$\rho = \frac{1}{N_D e \mu_e}$$

Where N_D is the concentration of donor atoms, e is the charge on the electron (1.6×10^{-19} C) and μ_e is the electron mobility which should be assumed to be $0.135 m^2/Vs$.

Calculate the resistivity of the n^--drift region and the required cross sectional area of the drift region such that the conduction loss in the device does not exceed 1 W/mm^2 at a rated current of 10 A. Assume the losses in the n^--drift region dominate the conduction losses.

[5]

New calculation. In this part of the question ρ means resistivity not charge density

Using the formulae given, the resistivity (ρ) is given by:

$$\rho = \frac{1}{N_D e \mu_e} = \frac{1}{1.6 \times 10^{20} \times 1.6 \times 10^{-19} \times 0.135} = 0.289 \Omega m$$

The losses in the device are given by:

$$P = I^2 R = I^2 \rho \frac{L}{A}$$

Thus the power dissipation is given as being 1 $W/mm^2 = 1 \times 10^6 W/m^2$:

$$\frac{P}{A} = I^2 \rho \frac{L}{A^2} = 1 \times 10^6$$

L, ρ and I are known, and thus:

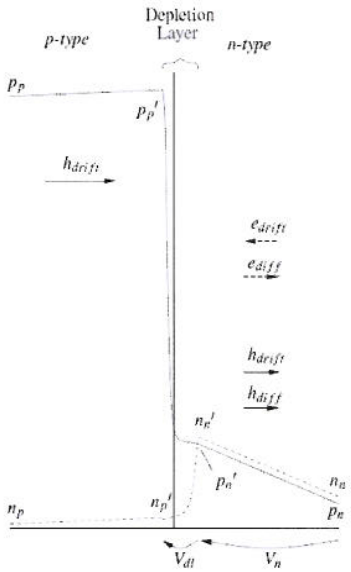
$$A = \sqrt{\frac{10^2 \times 0.289 \times 40 \times 10^{-6}}{1 \times 10^6}} = 3.4 \times 10^{-5} m^2 = 0.34 cm^2$$

iv) Explain how high-level injection in a simple p^+n diode causes additional conduction loss at a particular current to that predicted by the Shockley equation. Explain how a ***pin*** diode structure avoids this extra loss.

[5]

Bookwork:

The Schockley equation assumes that the diode is in low level injection. However, a p+n structure in forward bias has carrier concentrations as shown below and is operating in high level injection:



There is almost no electron current in the p+ region because there is almost no voltage across the p+ region and there are only very low diffusion gradients there. Consequently, for continuity of current there is almost no net electron current in the n region. High level injection in the n region causes a significant electron diffusion current which must be cancelled by a drift current. Therefore there is a significant voltage across the n region to cause an electron drift current to cancel electron diffusion current. Because a significant proportion of the applied diode voltage is present across the n region, this voltage is not available to be applied across the depletion layer. Consequently the increase in minority carriers concentration at the depletion layer edge is lower than predicted by the junction law because of the lower voltage across the depletion layer and so the current for a given applied voltage is less. Consequently, for a certain current to be achieved, more voltage is needed in a device operating in high level injection than the device in low level injection and thus the power loss is greater than predicted by the Shockley equation.

2. Consider the circuit of Figure 2, an IGBT switching an inductive load:

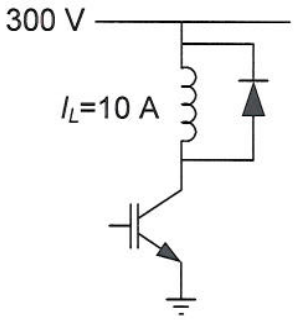


Figure 2 IGBT switching an inductive load

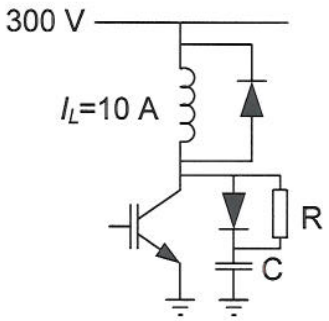
i) Explain how the inductively switched load gives rise to considerable switching loss in the transistor at turn off. Draw a diagram of a turn off snubber applied to this circuit and explain how the snubber can reduce the turn off loss.

[5]

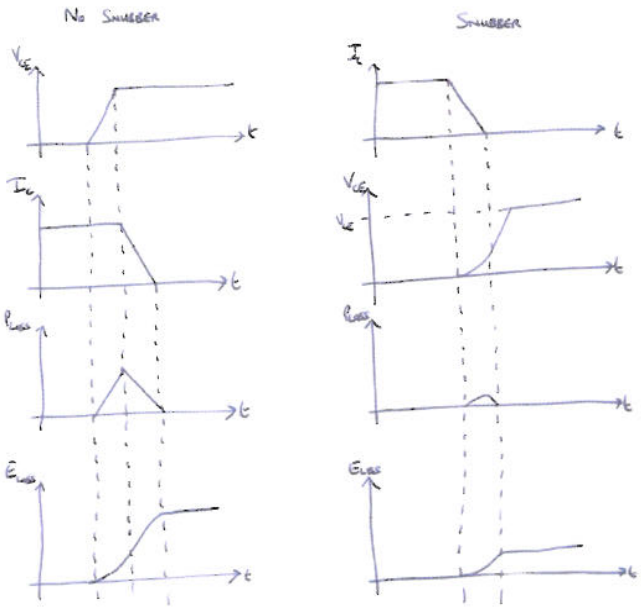
Bookwork:

Without the snubber:
At turn off, the inductor current forces the diode into conduction before the current in the IGBT can start to drop. This is because I_L is effectively constant over a switching period. This means V_{CE} must rise before I_C can fall. This means that without the snubber there is a considerable power loss because there is a considerable time when either the voltage or current is non-zero.

The circuit with a snubber looks as below:



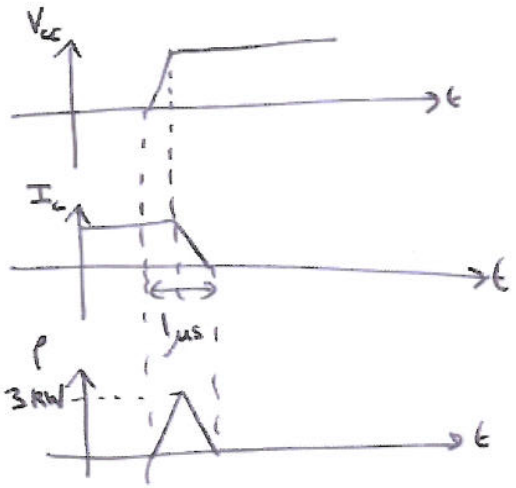
When a snubber is present, IC can fall whilst V_{CE} rises slowly, constrained to rise quadratically as the current falls. This significantly reduces the power and energy loss The waveforms are thus as shown overleaf:



ii) Assume a current fall time and voltage rise time of 0.5 μs each. Calculate the turn-off switching energy loss per cycle in the IGBT with an inductor current of 10 A and a supply voltage of 300 V.

[3]

Calculation:



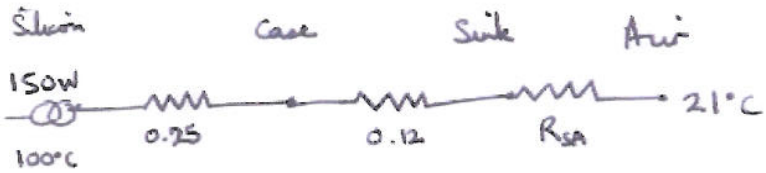
Peak power loss is 300 V ×10 A = 3 kW. Energy loss per cycle is thus $0.5\times3\text{ k}\times1\times10^{-6}=1.5\text{mJ}$

iii) For a room temperature of 21 °C and allowing a junction temperature of the IGBT of 100 °C, what should be the maximum thermal resistance between the heat sink and the air to cool the device at a switching frequency of 100 kHz?

What is the temperature of the heat sink under these conditions? Assume losses are dominated by turn-off losses, a thermal resistance between the silicon and case of 0.25 °C/W and the thermal resistance between the case and the heat sink is 0.12 °C/W

Heat sink calculation:

At 100 kHz, the total turn off losses is 150 W.



Newton's law of cooling gives:

$$150 = \frac{T1 - T2}{R_{total}} = \frac{100 - 21}{0.25 + 0.12 + R_{SA}}$$

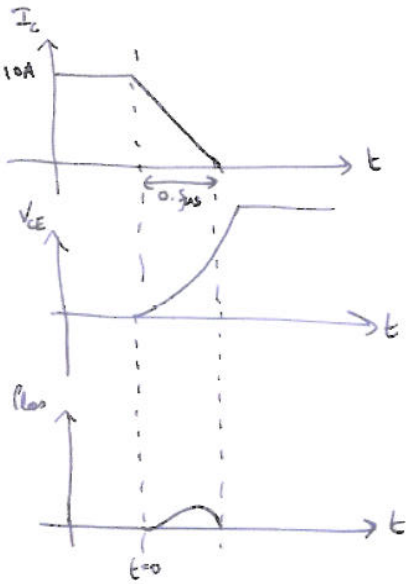
$$\therefore R_{SA} = 0.16^{o}C/W$$

The temperature difference between the sink and the air is thus given by $0.16 \times 150 = 44.5^{o}C$

iv) Design a snubber such that the turn off loss in the IGBT is reduced by a factor of 20. Assume the minimum duty cycle of the IGBT is 50 % and that the current falls linearly in a time of 0.5 μs.

[7]

The waveforms are as follows, remembering that V_{CE} is also the snubber capacitor voltage:



To decrease the turn off loss in the IGBT by a factor of 20 we require the switching loss to be reduced to 0.075 mJ.

Thus, we require:

$$E = \int_0^{0.5\mu} i_C(t) v_{CE}(t) dt < 0.075 \times 10^{-3}$$

The collector current is given by:

$$i_C(t) = 10 - 20 \times 10^6 t$$

Thus the snubber current is given by:

$$i_s(t) = 20 \times 10^6 t$$

Therefore:

$$V_{CE}(t) = \frac{1}{C} \int 20 \times 10^6 t dt$$

$$= \frac{1}{C} \times 10 \times 10^6 t^2$$

Thus, the energy dissipated in the IGBT during a turn off operation is:

$$E = \int_0^{0.5\mu} i_C(t) v_{CE}(t) dt$$

$$E = \int_0^{0.5\mu} (10 - 20\times10^6 t)\left(\frac{1}{C}\times10\times10^6 t^2\right)dt$$

$$E = \frac{10\times10^6}{C}\int_0^{0.5\mu}(10t^2 - 20\times10^6 t^3)dt$$

Thus:

$$E = \frac{10\times10^6}{C}\left[\frac{10t^3}{3} - \frac{20\times10^6 t^4}{4}\right]_0^{0.5\mu}$$

$$E = \frac{1.042\times10^{-12}}{C}$$

Thus for E=0.075mJ, C=13.8 nF

To calculate the resistance, at 100 kHz with a minimum duty cycle of 50%, the minimum on time is 0.5×10^{-5}s.

If we allow 5 time constants for snubber reset, then we require 5RC to be equal to 0.5×10^{-5}s.

This gives R=72.4Ω.

v) Calculate whether the circuit with the snubber is more or less efficient than the circuit without the snubber.

[2]

Calculation:

With the snubber, energy lost in switching is 0.075mJ. Energy stored in the snubber capacitor (which is lost at snubber reset) given by $\frac{1}{2}CV^2$

The final snubber voltage is 300 V and thus the energy stored is $0.5\times13.8n\times300^2=0.621mJ$

Therefore the total turn off loss is 0.621+0.075=0.696 mJ. This is more efficient than the circuit without the snubber where the loss was 1.5 mJ per switch off.

3.

a) Explain why the isolated Flyback converter is sometimes constructed with two MOSFETS rather than one. Comment on the voltage rating required of the MOSFET in each case. [4]

Single switched Flyback circuit has no path for primary current once the switch is off so energy in primary leakage inductance sets up oscillation with Mosfet output capacitance and causes large voltage overshoot and possible breakdown of the mosfet. Double-switched primary has diode path to discharge primary leakage energy. The two mosfets are an additional expense and circuit complexity but they are rated at only the input voltage. Single-switch circuit needs a mosfet rated at input voltage plus reflected output voltage plus the oscillatory overshoot.

b) Explain why the power factor of a simple diode rectifier is expected to be significantly less than unity. Comment on the consequences of this? [4]

Diode rectifiers draw input current only when instantaneous input voltage exceeds the DC voltage on the output capacitor. The conduction period is typically very brief and the current amplitude very large. This waveform has a very high harmonic distortion and very high RMS value compared to the fundamental component present. Since only the fundamental transmits active power, the power factor is very low, not because of phase displacement but because of distortion. The consequence are high heating effect in cables and transformers for a given power transmission. There are also consequent harmonic voltage drops in the lines and therefore common-impedance coupling of interference to other consumers.

c) Describe how the amplitude and frequency of the fundamental output of an inverter can be controlled. [4]

The reference to the modulator provides the means. By changing the amplitude and frequency of the reference the amplitude and frequency of the fundamental component of the inverter output is changed in a corresponding fashion. In a digital implementation, the rate at which the algorithm steps through the sinewave look-up table sets the frequency and a multiplier can be used to scale the look-up table result to control the amplitude.

d) Describe the relative merits of on-line and off-line forms of uninterruptible power supply. [4]

Off line

- Protects against outages and large magnitude, short duration voltage errors
- Only the low power rating 'trickle' charger is permanently connected to the mains and so standby losses are low
- Can not correct frequency errors, harmonic distortion or long term voltage magnitude errors

On line

- Provides full decoupling of input and output and can therefore correct frequency errors, harmonic distortion or long term voltage magnitude errors
- Requires fully rated rectifier
- Can also correct harmonic distortion of the load current if rectifier is unity power-factor design.
- Rectifier and inverter always processing full load power so standby efficiency is low.

e) Explain what is meant by four-quadrant operation of an electrical drive system and give examples of when operation in each quadrant is required. [4]

The four quadrants are those of the torque-speed plane. For instance positive torque and positive speed is the first quadrant and identifies the machine operating as a motor in the forward direction. To run as motor in reverse (reversing a conveyor belt for instance) requires third quadrant operation. If the load needs to be actively slowed down then torque in the opposite sense to speed is required and this is fourth quadrant for forward motion and second quadrant for reverse. This is regenerative breaking in which kinetic energy is recovered as electrical energy. A servo with a high inertia load requires this as does railway traction.

4.

(a) Explain why quasi-resonant circuits are sometimes used in switch-mode power supplies. [4]

The resonant circuit gives, for instance a turn-on process in which the current is constrained to be small and slowly increasing and a turn-off process which occurs with no current present in the switch. Thus power los during switching is either very low or zero. There is thus little or no penalty in increasing switching frequency and the benefits in passive component size of operating at high frequency can be realised.

(b) Figure 4.1 shows a zero-current switched quasi-resonant circuit and figure 4.2 shows the four periods of operation defined by the capacitor voltage and inductor current of the resonant circuit. Describe the circuit action in each of the four periods. [6]

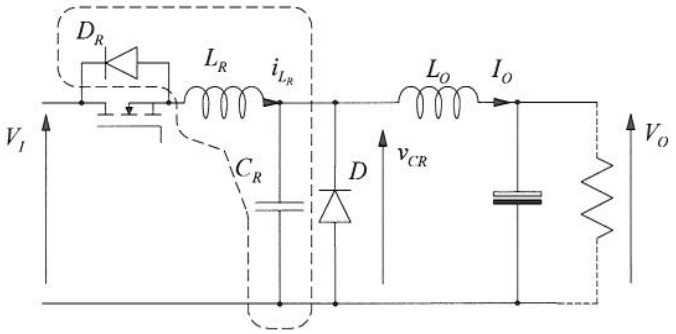


Figure 4.1 *A zero-current switched quasi-resonant circuit*

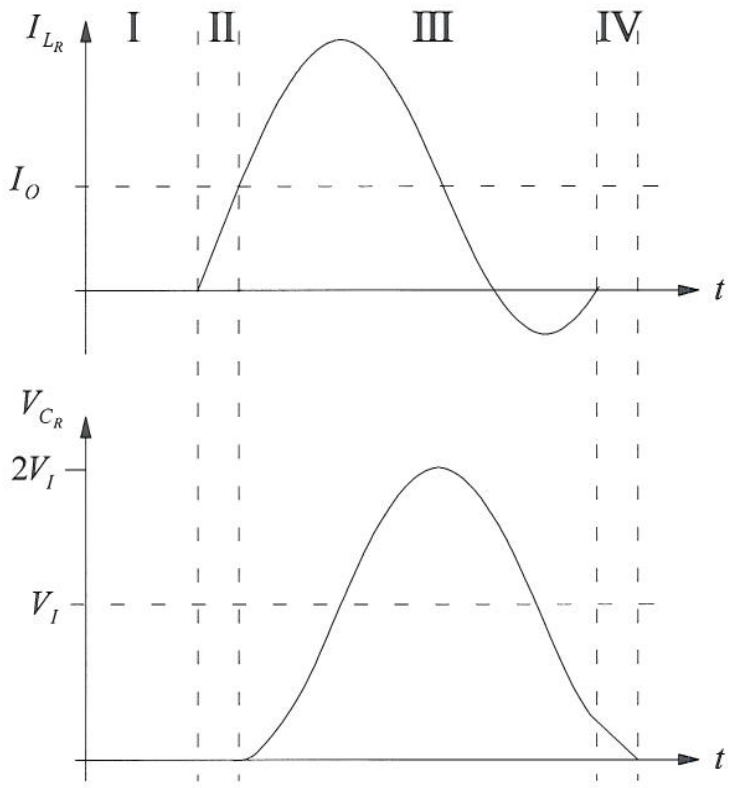


Figure 4.2 *The four periods of operations of a zero-current switched*

quasi-resonant circuit

Period I
The transistor is off and I_O flows in D. This state is stable.

Period II
The transistor is turned on and the input voltage is imposed across L_R. As a consequence i_{LR} rises linearly. D stays in conduction (and v_{CR} is held close to zero) because i_{LR} is less than I_O. This period lasts until $i_{LR} = I_O$.

Period III
D falls out of conduction and $L_R C_R$ form a resonant circuit governed by:

$$V_i = v_{C_r} + L_r \frac{d}{dt}\left(i_{C_R} + I_O\right)$$

$$= v_{C_r} + L_r C_r \frac{d^2 v_{C_r}}{dt^2}$$

with initial conditions of $i_{LR} = I_O$ and $v_{CR} = 0$.

The solution to this differential equation yields:

$$i_{L_R} = I_O + \frac{V_I}{\omega_R L_R} \sin(\omega_R t)$$

$$v_{C_R} = V_I \left(1 - \cos(\omega_R t)\right)$$

$$\text{where } \omega_R = \frac{1}{\sqrt{L_R C_R}}$$

Period III ends when the i_{LR} rises again to zero but is blocked from becoming positive because the transistor is off.

Period IV
When period III ends there is residual charge on C_R that is discharged (linearly) by the continued flow of I_O. This period ends when v_{CR} reaches zero and D is brought into conduction. The circuit then re-enters the stable state I.

If period IV is short then the average voltage during period III is V_I

(c) A circuit is to be designed for $V_I = 24$ V, $V_o = 10$ V and $I_o = 1$ A. It has already been decided that the resonant frequency of the C_R and L_R combination will be 250 kHz. Find the overall period with which the circuit will need to be operated. [3]

You may use the result that during period III the circuit is governed by the equations:

$$i_{L_R} = I_o + \frac{V_i}{\omega\ L_R}\ \sin(\omega\ t\ )$$

$$v_{C_R} = V_i\ \left(1 - \cos(\omega\ t\ )\right)$$

Assuming period IV to be brief the average voltage applied in period III to the output is V_I

$$V_O = \frac{\int_0^{t_{III}} V_I\left(1-\cos(\omega_R t)\right).dt}{t_I + t_{II} + t_{III} + t_{IV}}$$

$$\approx V_I \frac{t_{III}}{T}$$

$$T = \frac{V_I}{V_O}\cdot\frac{1}{f} = \frac{24}{10}\cdot\frac{1}{250\times10^3} = 9.6\ \mu s$$

(d) Mark on a sketch of the graph of i_{LR} the limits of the period during which the transistor can be switched off under zero current conditions. [2]

Identify period as sub-period of period III in which i_{LR} is negative.

(e) It is desired to have at least a 200 ns period in which to turn off-the transistor. State the angle that this time represents with respect to the resonant cycle of C_R and L_R. Choose a value of L_R, and hence C_R, to achieve the desired turn-off window. [5]

$$\theta_{Off\_Window} = 360° \times \frac{t_{Off\_Windon}}{T} = 360° \times 200\times10^{-9} \times 250\times10^3 = 18°$$

The turn-off window begins when i_{LR} crosses zero:

$$i_{LR} = 0 \Rightarrow \sin(\omega_R t) = -\frac{I_O}{V_I / \omega_R L_R}$$

$$L_R = -\frac{V_I}{\omega_R I_O}\sin\left(270° - \tfrac{1}{2}\times18°\right) = -\frac{24}{2\pi\times250\times10^3\times1.0}\times\sin\left(270° - \tfrac{1}{2}\times18°\right) = 15\ \mu H$$

$$C_R = \frac{1}{\omega_R^2 L_R} = \frac{1}{\left(2\pi\times250\times10^3\right)^2\times15\times10^{-6}} = 26.9\quad nF$$

5.

(a) Compare and contrast the Cúk and buck-Boost switch mode power supplies, SMPS.

Both provide a reverse polarity output voltage that can be greater or less than the magnitude of the input voltage according to the relation $\frac{V_O}{V_I} = \frac{-\delta}{1-\delta}$ .in continuous operation.

The Cúk converter has an extra inductor and an extra capacitor. The advantage these bring is that both the input and output currents flow in inductors and thus if the inductor currents are maintained in continuous conduction then the input and output currents can be designed to have vary low ripple values. For EMC compliance and low output voltage ripple the Cúk converter has advantages. The buck-boost converter is a lower cost circuit.

[5 marks]

(b) Derive the relationship between input and output voltage for the Cúk SMPS.

We assume that the capacitors are sufficiently large such that the voltages across them do not change significantly during a switching cycle. We further assume that the inductors are in continuous conduction and that resistive and semiconductor voltage drops are negligible. The rise and fall of current in the inductors can be found and the assumption of steady-state applied.

$$\Delta i_1(on) = \frac{V_I}{L_1} \cdot \frac{\delta}{f} \qquad \Delta i_1(off) = \frac{V_I - V_{C1}}{L_1} \cdot \frac{1-\delta}{f}$$

$$\Delta i_1(on) + \Delta i_1(off) = 0$$

$$\frac{V_{C1}}{V_I} = \frac{1}{1-\delta}$$

$$\Delta i_2(on) = \frac{V_O + V_{C1}}{L_2} \cdot \frac{\delta}{f} \qquad \Delta i_2(off) = \frac{V_O}{L_2} \cdot \frac{1-\delta}{f}$$

$$\Delta i_2(on) + \Delta i_2(off) = 0$$

$$\frac{V_O}{V_{C1}} = -\delta$$

$$\frac{V_O}{V_I} = \frac{-\delta}{1-\delta}$$

[5 marks]

(c) A power supply is to be designed that is subject to size constraints and voltage ripple tolerance. The outline specification is for conversion of +15V to -5V at an output current of 2A.

(i) Calculate the current flowing in the inductor of the flyback SMPS and both inductors of the Cúk SMPS.

Buck – boost

$$I_O = I_D(average) = I_L(1-\delta)$$

$$\delta = \frac{V_O}{V_O - V_I} = \frac{-5}{-5-15} = 25\%$$

$$I_L = \frac{2}{(1-0.25)} = 2.67\,A$$

Cuk

$$I_{L2} = I_O = 2\,A$$

$$V_I I_{L1} = -V_O I_{L2}$$

$$I_{L1} = -I_{L2}\frac{V_O}{V_I} = \frac{-2\times -5}{15} = 0.667\,A$$

[5 marks]

(ii) Given the constraint that the LI^2 of the inductors is limited to 10^{-3} HA^2 for the Buck-boost and $0.5x10^{-3}$ for each inductor in the Cúk, calculate the value of the inductors. Calculate the peak-to-peak ripple current flowing in the input of each SMPS and the peak-to-peak output voltage ripple if the output capacitor has an effective series resistance of 40mΩ and the switching frequency is 40 kHz.

Buck – boost

$$L = \frac{10^{-3}}{2.67^2} = 0.14\,\text{mH}$$

$$\Delta i_L = \frac{V_I}{L}\cdot\frac{\delta}{f} = \frac{15\times 0.25}{0.14\times 10^{-3}\times 40\times 10^3} = 0.67\,A$$

$$I_I(ptp) = \hat{i}_L = I_L + \Delta i_L = 2.67 + 0.67 = 3.33\,A$$

$$V_O(ptp) = \hat{i}_L R_{ESR} = 3.33\times 0.04 = 133\,\text{mV}$$

Cuk

$$L_1 = \frac{0.5\times 10^{-3}}{0.667^2} = 1.125\,\text{mH}$$

$$L_2 = \frac{0.5\times 10^{-3}}{2^2} = 0.125\,\text{mH}$$

$$I_I(ptp) = \Delta i_{L1} = \frac{V_I}{L_1}\cdot\frac{\delta}{f} = \frac{15\times 0.25}{1.125\times 10^{-3}\times 40\times 10^3} = 0.083\,A$$

$$\Delta i_{L2} = \frac{V_O}{L_2}\cdot\frac{1-\delta}{f} = \frac{5\times(1-0.25)}{0.125\times 10^{-3}\times 40\times 10^3} = 0.75\,A$$

$$V_O(ptp) = \Delta i_2 R_{ESR} = 0.375\times 0.04 = 30\,\text{mV}$$

[5 marks]

6)

(a) Describe the operation of a brushless DC motor. Provide block diagrams of the systems and a sketch of the power converter circuit.

[7 marks]

Brushless machine has a permanent magnet rotor and a wound stator. The stator is typically windings which have trapezoidal back-emf. The stator is fed with regulated current. The polarity of current in each winding is set according to the whether the winding is in the north or south pole field of the rotor. Consequently, as the rotor rotates the polarities of the stator currents are changed in synchronism. This requires measurement of the absolute rotor position. The amplitude of the stator current can be set to control the torque developed. The power converter is a voltage source device with current feedback.

Diagrams as in notes.

(b) Compare the power converter circuit to the power converter circuit required for a traditional (brushed) DC motor to be operated in forward and reverse rotation with braking and accelerating torque.

[4 marks]

Diagram of 4-transistor (4 quadrant) chopper required. A typical brushless-dc drive will have 6 transistors compared with 4 for the brushed design. The extra cost, not least of the extra high-side driver is a disadvantage but it is only a 50% increase in semiconductor numbers for the advantage of no brush gear. Both circuits would normally be used in current feedback control. The brushless form requires 3 current sensors compared to one in the brushed form.

(c) Justify the shape of the torque speed diagram in figure 6 with respect to a dc machine. Calculate the principal points on the diagram for a system with the following properties:

DC input voltage 100 V
Armature resistance 0.5 Ω
Field flux at maximum field current 18 mWb
Armature constant 12.5 $V.s.rad^{-1}.Wb^{-1}$ (or $N.m.A^{-1}.Wb^{-1}$)
Rated armature current 8 A

[5 marks]

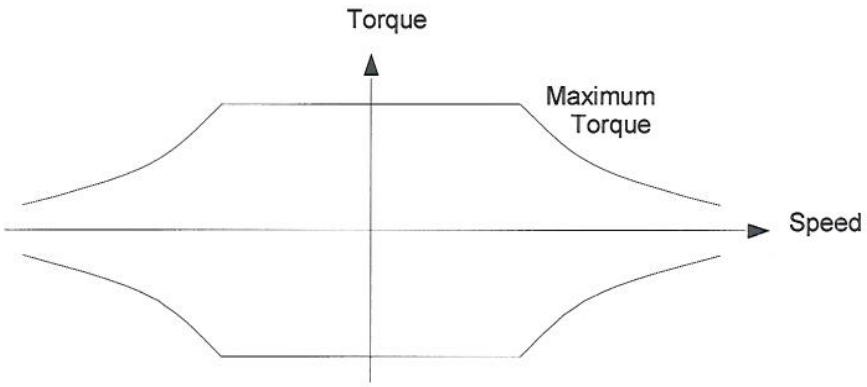


Figure 6 A typical torque speed diagram of an electrical drive system

Torque is proportional to current and flux. Under constant flux conditions the maximum torque achieved is limited by the current rating of the machine and is independent of speed (or direction). By reversing the current, reverse torque can be achieved.

$$T_{\max} = I_{\max}\phi_{\max}k_a = 8 \times 0.018 \times 12.5 = 1.8 \text{ Nm}$$

As speed increases, the back EMF of the machine increases. Eventually a point is reached where the back EMF is equal to the maximum available supply voltage and it is no longer possible to maintain the desired current flow. Beyond this point the field current is reduced to reduce the flux. The fall in flux reduces the back EMF and allows current control to be maintained but causes a reduction in available torque. Flux is decreased in inverse proportion to the speed so as to maintain the back EMF constant. Therefore the torque available becomes inversely proportional to speed.

The maximum speed at which maximum torque is available is:

$$\omega_{base} = \frac{V_{\max}}{\phi_{\max}k_a} = \frac{100}{0.018 \times 12.5} = 444 \text{ rad/s or } 4244 \text{ rpm}$$

more accurately:

$$\omega_{base} = \frac{V_{\max} - I_{\max}R_a}{\phi_{\max}k_a} = \frac{100 - 0.5 * 8}{0.018 \times 12.5} = 426 \text{ rad/s or } 4074 \text{ rpm}$$

The same speeds can be achieved in reverse.

(d) Summarise the relative merits of brushed and brushless DC drive system. [4 marks]

Brushless form:

- *does not require regular maintenance*
- *does not have arcing and EMC problems of commutation*
- *does not have field current power loss*
- *requires 6 transistors, position sensor and current sensor*

Brushed form:

- *can be operated with single transistor chopper if only positive speed and torque required.*
- *can be operated open loop (in terms of speed, current or both) in undemanding applications*
- *brush gear requires significant extra volume in small machines.*