Paper Number(s): **E3.02**
AM4

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2000

MSc and EEE PART III/IV: M.Eng., B.Eng. and ACGI

INSTRUMENTATION

Thursday, 18 May 2000, 10:00 am

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks.

Corrected Copy

Time allowed: 3:00 hours

Examiners: Dr A.J. Payne, Dr C. Papavassiliou

1. (a) Various sensors are available which produce an output variation in response to some change in input, including the measurement of (i) temperature, (ii) strain, (iii) light, (iv) position. Describe (with the aid of diagrams where appropriate) a possible sensor for the measurements (i)-(iv) above, outlining in each case the basic operation of the sensor, and how it should be configured to perform the required measurement.

(b) A resistive temperature detector (RTD) is used as one arm of a Wheatstone Bridge. The RTD has a resistance of 280 Ω at 25 °C and a temperature coefficient (assumed to be linear) of 0.5 Ω/°C. The other three arms of the bridge contain dummy resistors of value 280 Ω, with a bridge supply voltage of 10 V. Calculate the expected bridge output voltage at 77 °C. In practice the output voltage magnitude at 77 °C is measured to be 0.2 V. If this error is assumed to be due to the temperature variation of the dummy resistors, calculate the first order temperature coefficient of the dummy resistors (you may assume that the dummy resistors are at the same temperature as the RTD, and the nominal dummy resistor value of 280 Ω was measured at 25 °C). It is later discovered that the dummy resistors have a temperature sensitivity of 2.5×10^{-4} (quoted relative to the nominal 280 Ω). The remaining error is attributed to the second order temperature sensitivity of the RTD, hence calculate the second order temperature coefficient of the RTD.

2. (a) A digital sampling oscilloscope (DSO) samples the analogue input waveform at a maximum rate of 500 M/s, and saves these samples in memory for subsequent processing and display. Outline why sampling a signal at the Nyquist rate is likely to lead to a distorted output on the DSO screen, if the resulting samples are directly displayed. Describe how the technique of interpolation is used to overcome this distortion, and calculate the approximate maximum input signal frequency which can be displayed without significant distortion if the DSO uses (i) no interpolation, (ii) linear interpolation, (iii) sine interpolation.

(b) Explain how the process of sampling may distort the spectrum of the sampled signal, and calculate the attenuation of a 500 kHz signal which is sampled at 3 MHz. Outline how a reconstruction filter may be used to eliminate this distortion.

(c) The DSO described above is used to perform an ensemble average to recover a periodic signal which is obscured by white noise. The periodic signal has an rms amplitude of 220 μV and frequency 5 MHz, while the rms amplitude of the noise is 7 mV. The DSO sampling frequency is set to the maximum value. If the analog-to-digital converter (ADC) within the DSO has a resolution of 10 bits, calculate the number of sampling periods required to give a final signal-to-noise ratio of 25 dB. If the ADC adjusts its gain such that the samples always exploit the full dynamic range, calculate the minimum total memory required to perform the ensemble average, and the time taken to perform this average.

3. (a) An integrated circuit (IC) digital-to-analogue converter (DAC) is implemented using weighted current sources as shown in *Figure 3a*. Outline the purpose of the lower devices and explain why it is necessary to use asymmetrical switching signals B/BN. The matching of the DAC current sources is required to be better than +/- 0.5 LSB. Calculate the required matching accuracy of the DAC MSB current source if this architecture is extended to implement (i) an 8-bit DAC, (ii) a 12-bit DAC.

(b) The dynamic performance of a weighted current-source DAC can be improved by using thermometer decoding. Briefly describe the principle of operation of a thermometer-decoded current-source DAC, and give one disadvantage of this method.

(c) An analogue input signal is to be digitised using the system shown in *Figure 3b*. The maximum input signal frequency is 35 kHz, and the analogue-to-digital converter (ADC) sampling frequency is 100 kHz. The sample-and-hold circuitry is used to maintain a constant input signal to the ADC while the conversion takes place. The ADC is an 8-bit converter which is adjusted to ensure that the maximum input signal fills all levels of the converter. Calculate:

(i) the maximum acquisition time of the sample-and-hold circuit, if the sampling error is to be less than 0.5 LSB,

(ii) the maximum ADC conversion time

(iii) the minimum order of the antialiasing filter, if aliasing errors are to be less than 0.5 LSB.

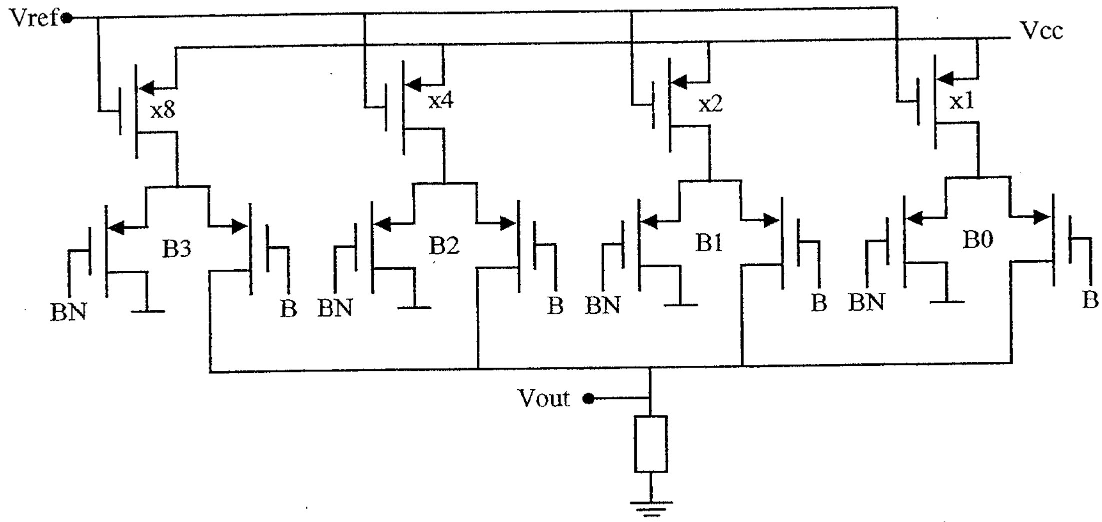


Figure 3a

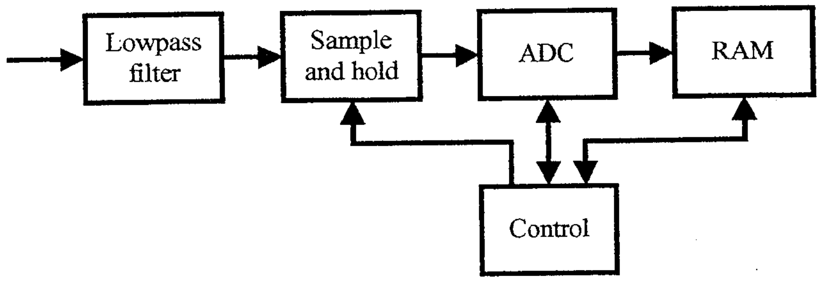


Figure 3b

4. (a) *Figure 4* shows a circuit used to perform frequency-to-voltage conversion. Outline the operation of this circuit, and choose a suitable value for the sawtooth waveform slope given that the minimum input signal frequency is 200 Hz. You may assume that the maximum output signal from the sawtooth waveform generator is 10 V.

(b) The output voltage from this f-to-v converter is to be subsequently digitised. If a 10-bit analogue-to-digital converter (ADC) is available, calculate the minimum change in period which can be detected. Hence comment on the frequency resolution of the system at an input frequency of (i) 200 kHz, (ii) 500 Hz.

(c) Interference signals may be coupled into a circuit and corrupt the signal of interest. Describe how this problem is reduced by using balanced signals or by shielding. Show with the aid of a diagram how both of these techniques may be combined for very low level signal measurements.

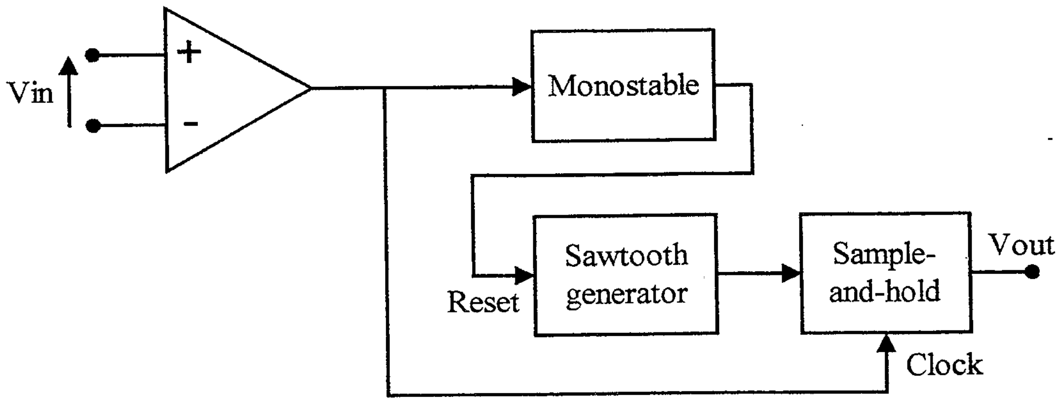


Figure 4

5. (a) *Figure 5* shows a circuit designed to measure temperature. Derive an expression showing how the output voltage varies with temperature, and hence choose suitable values for R1 and R2 to give an output voltage sensitivity of 0.1 V/°C, given that V_{be} = 0.68 V at T = 27 °C, and $\frac{dV_{be}}{dT}$ = -2.1 mV/°C. The output voltage at 0 °C should be 0 V.

(b) In practice the reference current I_{ref} may vary by up to 10 %. Calculate the resulting maximum error voltage at 0 °C due to this current uncertainty, and determine the tuning range of R2 required to null this offset voltage. What will be the variation in output sensitivity as R2 is tuned over this range? Show how the circuit could be modified to allow the output voltage at 0 °C to be nulled by a single resistor without altering the gain of the circuit.

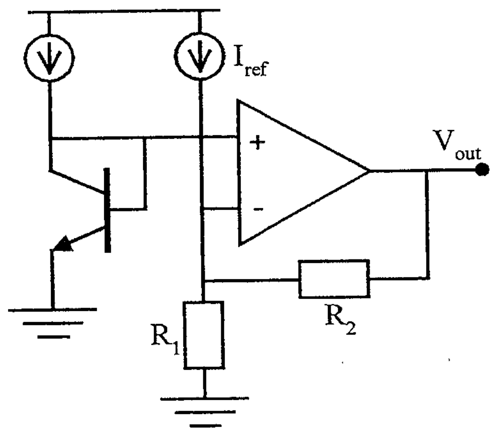


Figure 5

(c) Show mathematically that the amplitude and phase of a sinusoidal signal buried in noise can be recovered by cross-correlating it with a signal of an appropriate frequency, and give a block diagram suggesting how this may be implemented in practice. If the frequency of the required signal is not known, suggest how this technique could be modified to allow the signal frequency to be determined.

6. (a) *Figure 6a* shows the block diagram of a phase-locked loop (PLL), which is implemented using a commercial IC (the 4046A PLL plus VCO) with an external loop filter. Derive an expression for the (small-signal) closed loop transfer function of this PLL, given that a simple first order lowpass filter is used. Given that the type 1 phase detector is to be used, and with reference to the 4046A data sheet extracts (*Figures 6b, 6c*), calculate appropriate values for the following components (you may assume V_{CC}=5 V, VCO gain $K_V = \frac{4\pi f_L}{V_{CC}}$ rad s^{-1} V^{-1}, phase detector gain $K_D = \frac{V_{CC}}{\pi}$ V r^{-1}):

(i) VCO resistor and capacitor values to give a lock rage $2f_L$ = 350 kHz and frequency offset 250 kHz.

(ii) Filter component values to give a natural (loop) frequency ωn =100 kHz

With these component values, what is the resulting damping factor ζ of the loop? Comment briefly on the capture range and frequency stability of the resulting PLL, and calculate an approximate value for the voltage ripple at the VCO input when the input signal frequency is 250 kHz.

(b) *Figure 6d* shows a PLL with a dual modulus frequency divider used to implement a 'fractional-N' frequency synthesiser. The frequency divider is switched between its two different values by the control signal (CTL), such that the divide ratio = 8 when CTL is low, and divide ratio = 9 when CTL is high. Given that the reference signal frequency is 1 MHz, calculate the resulting average VCO output frequency if the periodic CTL signal is low for 20 cycles of the VCO output and high for 3 cycles of the VCO output. Sketch a rough diagram of the frequency spectrum of the VCO output signal.

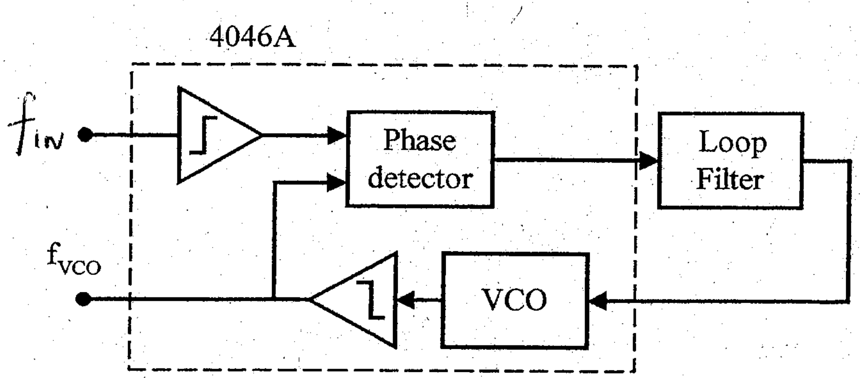


Figure 6a

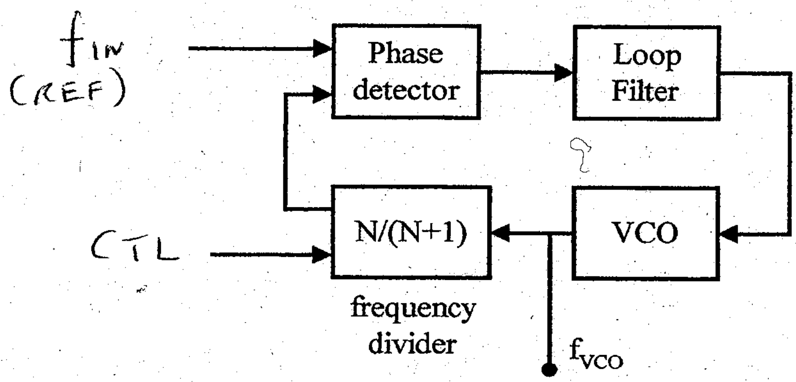
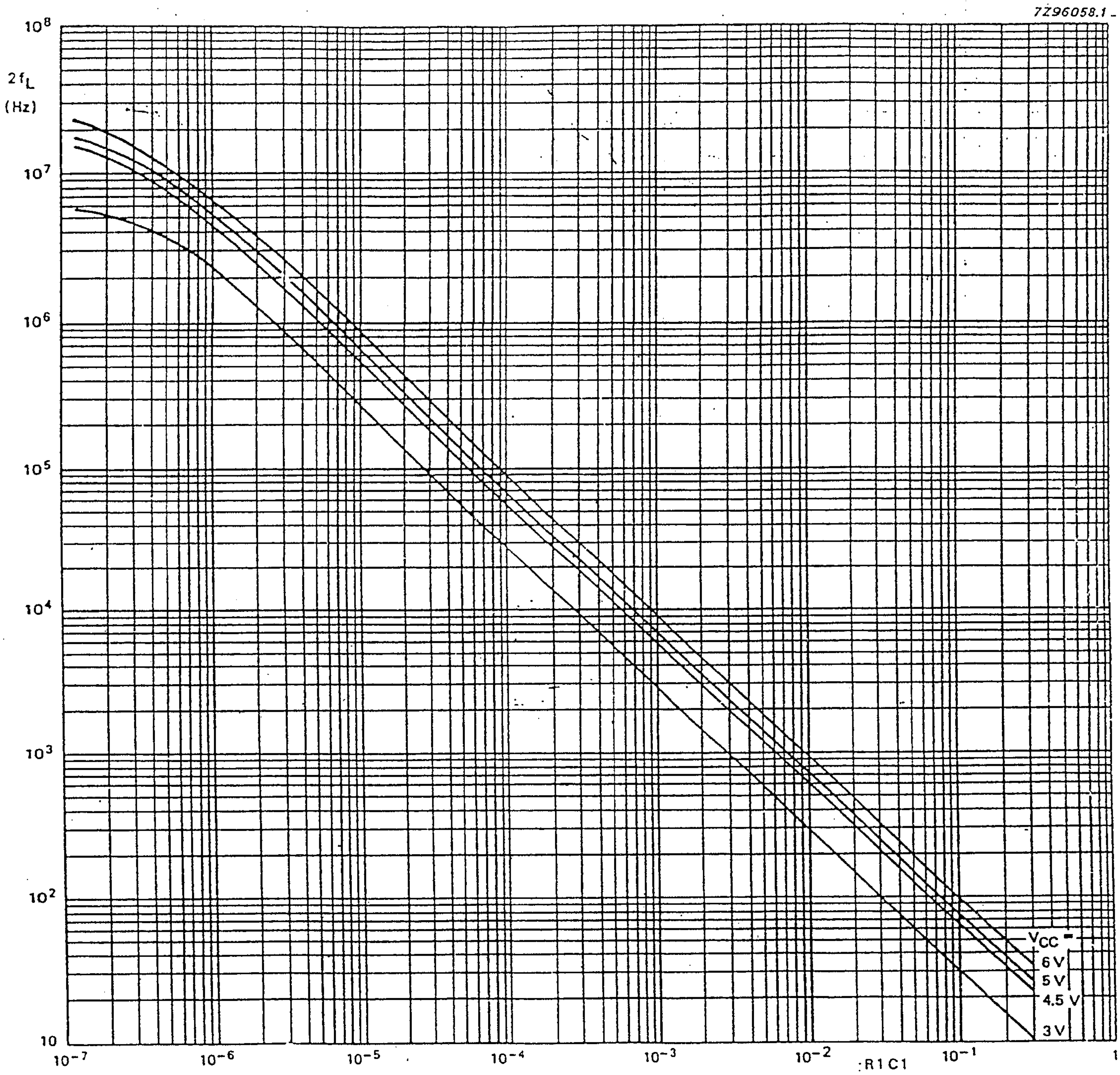
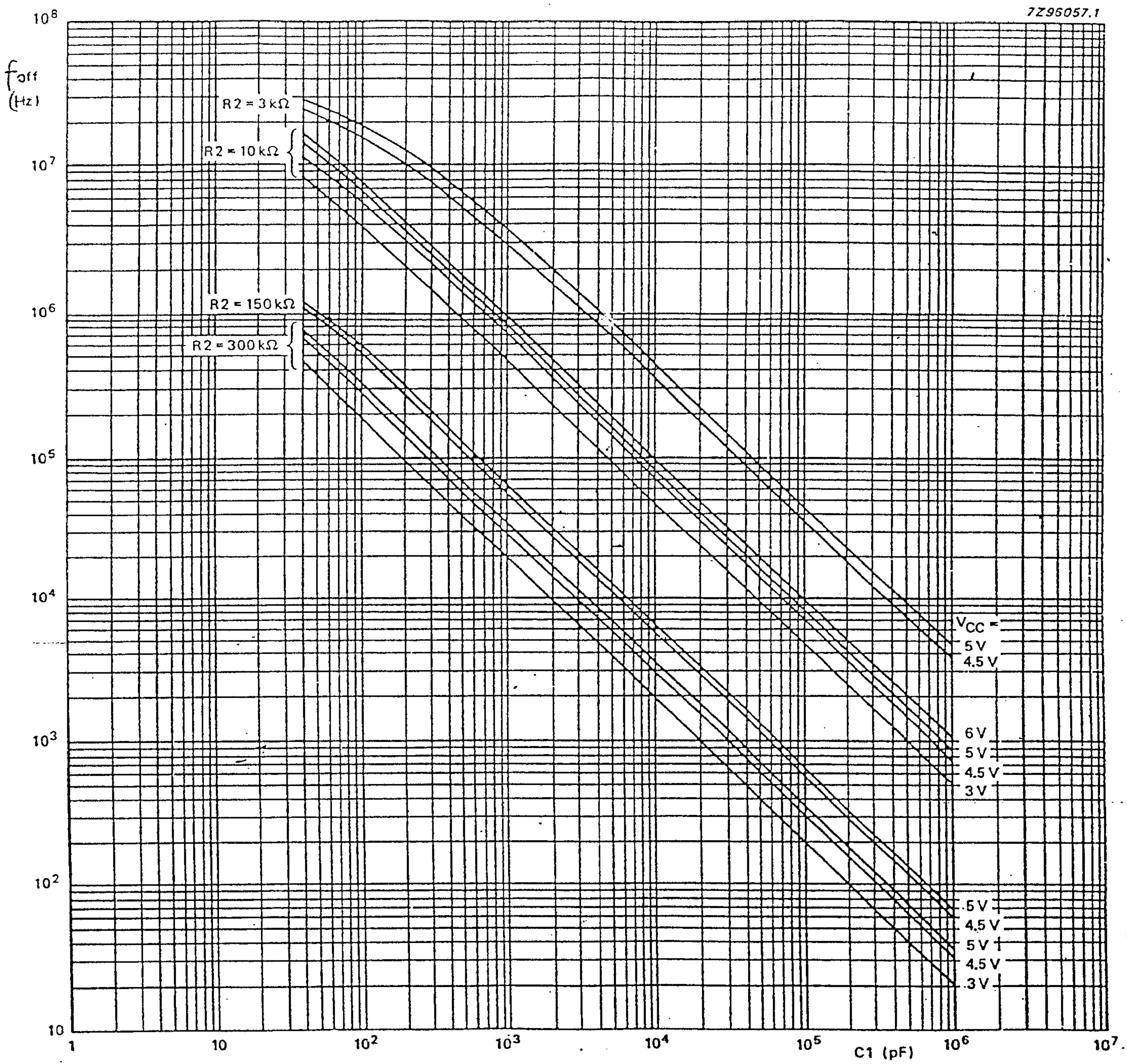


Figure 6d



Typical VCO frequency lock range ($2f_L$) versus the product R1C1

Figure 6b



Typical value of frequency offset as a function of C1

Figure 6c

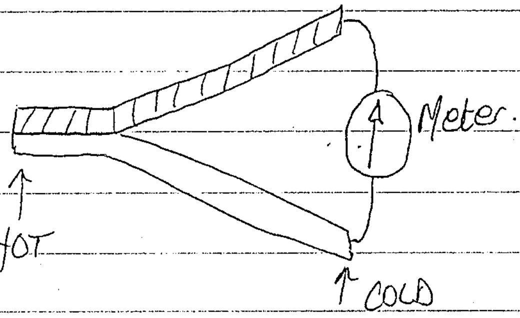
1

(i) Temperature – any one of the following is OK:

- Resistive temp detector (RTD): metallic, often platinum, fairly linear, positive tempco, $R_T = R_{T0}(1 + \alpha T)$
Usually used as one arm of Wheatstone bridge.

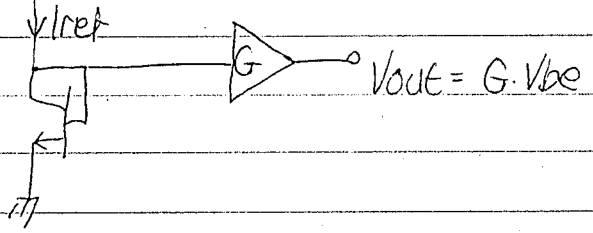
- Thermistor: generally non-linear change in resistance with negative tempco, $R = R_0 \exp B(T^{-1} - T_0^{-1})$
Usually used as one arm of Wheatstone bridge

- Thermocouple:



2 dissimilar metals joined at on end. A voltage appears across thermocouple which is proportional to temp. difference between the two ends (Seebeck effect). Must usually be calibrated by a more accurate temp sensor. Can withstand high temperatures.

- Solid state temperature sensor: The Vbe of a BJT is inversely proportional to temp given a constant collector current, typically $-2mV/°C$. Either measure this directly:

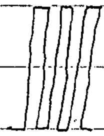


or measure the temp. difference between two BJTs with different emitter areas:

$$\Delta V_{be} = V_{be1} - V_{be2} = V_T \ln\left\{\frac{I_{C1} \cdot A_2}{I_{C2} \cdot A_1}\right\} = \frac{KT}{q} \ln(A_2/A_1)$$

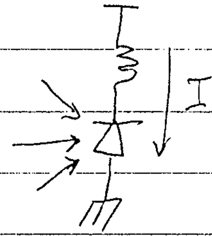
if $I_{C1} = I_{C2}$, i.e proportional to absolute temp. 3

(ii) Strain: A strain gauge is a piezo-resistive element whose resistance changes as force is applied. Tension causes an increase in length & a decrease in cross-sectional area, thus resistance increases (vice versa for compression). A zig-zag structure is typical:



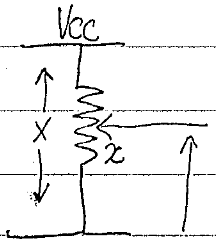
Generally used as one or more arms of a Wheatstone bridge 3

(iii) Light
A photodiode increases its reverse (leakage) current when illuminated, due to the creation of extra hole-electron pairs.



A phototransistor is a BJT whose collector current flows when the base region is illuminated. The output current is typically higher than in a photodiode due to the amplification by β. 3

(iv) Motion
eg. potentiometer displacement transducer:

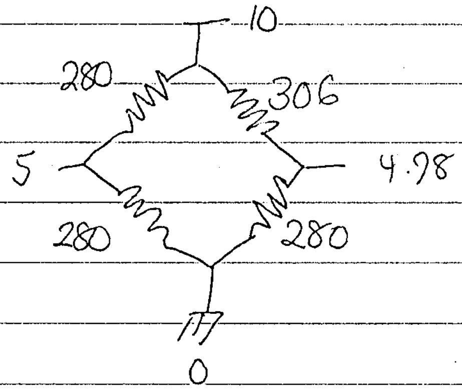


$V_{out} = V_{cc} \cdot \frac{x}{X}$

Wiper is moveable (eg attached to joystick). 3

$RTD = 280 + 0.5(T-25)$

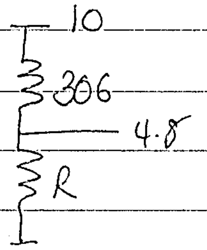
At 77°, $RTD = 306\,\Omega$



$V_{out} = \pm 0.22V$ at 77°

(4)

In practice $V_{out}(77^{\circ}) = 0.2V$



$$\frac{R}{R+306} \cdot 10 = 4.8$$

$$5.2R = 306 \times 4.8$$

$$R = 282.5$$

Thus $282.5 = 280 + T_c(77-25)$

$T_c = 0.05\,\Omega/^{\circ}C$

(4)

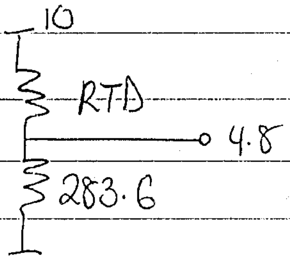
In practice, $S_R^T = 250$ ppm $= 0.00025$

$$S_R^T = \frac{1}{R}\frac{dR}{dT} \quad \therefore \frac{dR}{dT} = 25\times10^{-4} \cdot 280$$

$$= 0.07$$

$\therefore R = 280 + 0.07(T-25) = 283.6\,\Omega$ at 77°.

4/20



$$4.8 = \frac{283.6}{RTD + 283.6} \cdot \times 10$$

$$RTD = 307.2\,\Omega$$

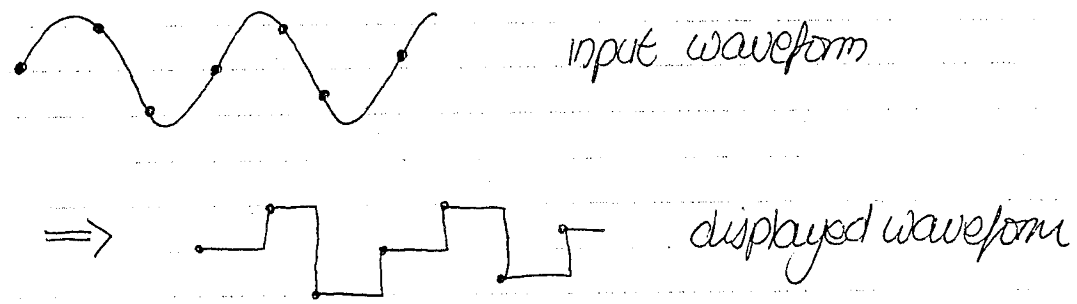
$$307.2 = 280 + 0.5(T-25) + x(T-25)^2$$

$$= 306 + x(T-25)^2$$

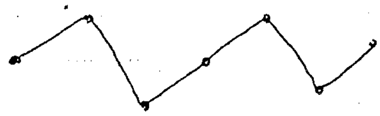
X = 2nd order tempco = $4.43 \times 10^{-4}\ \Omega/°C$. 5

TOTAL = 25

② If no additional information is provided, the DSO is likely to display & hold the waveform samples, leading to a distorted output:



The DSO must somehow 'fill in' the waveform between sampling instants. This is known as interpolation. The most simple method is linear interpolation:



④

More complex interpolation schemes are used in practice.

(i) No interpolation: ≃ 25 samples per period

(ii) Linear interpolation ≃ 10 samples per period

(iii) Sine interpolation ≃ 2.5 samples per period

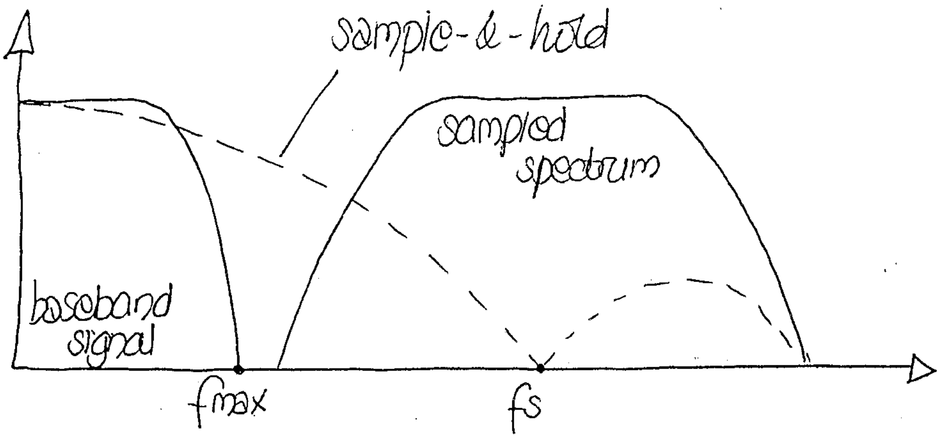
∴ maximum signal frequency

(i) 20 MHz (ii) 50 MHz (iii) 200 MHz ③

Interpolation gives a 1 period delay, as interpolated values are calculated from current & following samples.

A sample-&-hold circuit has a $\sin x/x$ frequency response, since while it is holding the sampled signal it is unable to respond to changes in the input until the next sample.

This frequency response may shape the spectrum of the sampled signal, especially if we sample close to the Nyquist frequency:



(4)

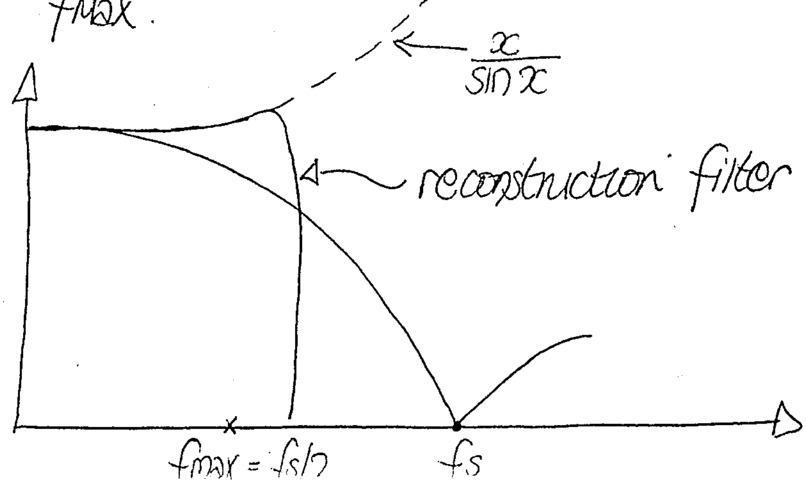
$$S/H \text{ spectrum} = \frac{\sin x}{x} \quad \text{where } x = \frac{\pi f}{fs}$$

$$\Rightarrow \text{Attenuation} \Rightarrow \frac{\sin(500K \cdot \pi/3M)}{[500K \cdot \pi]/3M} = \frac{0.5}{0.52} = 0.96$$

Attenuation = 4% (2)

A reconstruction filter corrects for the $\sin x/x$ attenuation by providing an opposite ($x/\sin x$) response.

Since $x/\sin x$ will rise to infinity at some frequencies, the reconstruction filter usually has a sharp roll off above fmax.



(3)

Initial SNR = $\frac{220\mu}{7m}$ = 31.4×10^{-3}

Final SNR = $10^{25/20}$ = 17.78

$\therefore$ $\sqrt{N}$ = $\frac{17.78}{31.4 \times 10^{-3}}$ = 566.2

N = 320 630 samples (ensembles)

3

signal freq = 5 MHz
Sampling freq = 500 MHz

$\therefore$ 100 samples per period

Initially, noise fills the converter : LSB = $\frac{7 mV}{2^{10}}$

= 6.84 μV

After 320 630 complete periods, signal will dominate.
$\therefore$ Memory required :

220μV × 320 630 = 70.5V

= 10 307 017 LSBs

= 24 bits 3

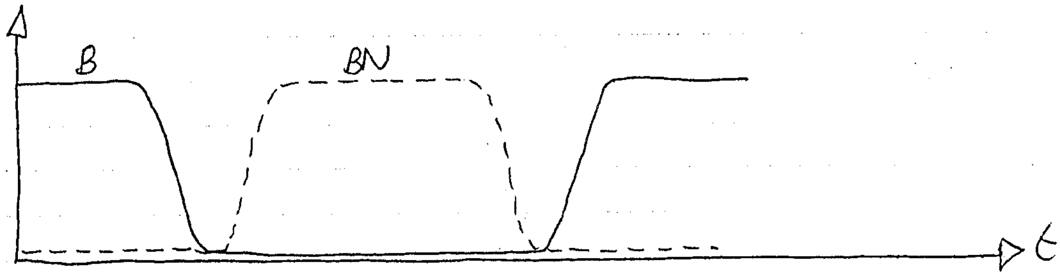
~~22~~ 24 bits per sample × 100 samples per period = 2400 bits

ensemble time = 320 630 × $\frac{1}{5M}$ = 64 mS 3

TOTAL = 25

Q3 The lower transistors are used as current steering switches, which direct the current either to the output or to ground.
These switches enable a constant current to be drawn from the supply, since the current source does not need to be switched on & off. This in turn reduces power supply variations / glitches. (3)

We must ensure that both steering switches do not turn off simultaneously, as this would 'saturate' the current source causing a longer switching time. Thus asymmetrical drive signals are used to ensure 'make before break' operation.



(3)

DNL must be within ± 0.5 LSB,

(i) 4-bit DAC, matching within $\frac{0.5}{8} \times 100 = 6.25\%$

(ii) 8-bit DAC, matching within $\frac{0.5}{128} \times 100 = 0.39\%$

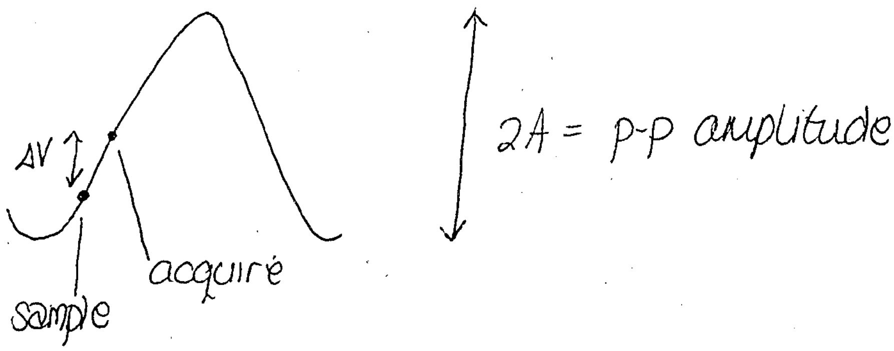
(iii) 12-bit DAC, " " $\frac{0.5}{2048} \times 100 = 0.02\%$. (2)

With a weighted current source array, there are likely to be large glitches when switching. eg going from 01111111 → 10000000 we may pass through the full-scale output 11111111.

To eliminate this problem, we implement the DAC using 2^N equal sized current sources. The thermometer decoder ensures that we only ever switch ON current sources if the input is increasing, or switch OFF current sources if the input is decreasing. i.e. we never switch sources on & off when the input changes, thus we avoid overshoot (glitches). (3)

Disadvantage of thermometer decoding: larger area required for digital decoder than a simple weighted current source DAC. (1)

(i)



Require $\Delta V < 0.5\,LSB$

Input signal $= A\sin(2\pi f t)$

$$\frac{\partial V_{in}}{\partial t} = 2\pi f A\cos(2\pi f t)$$

$$\partial V_{in}/\partial t\big|_{max} = 2\pi f_{max}\cdot A$$

$$\therefore \Delta V = 2\pi f_{max}\cdot A\cdot t_{acq}$$ t_{acq} = S/H acquisition time

$$LSB = \frac{2A}{2^N-1} \qquad \therefore 2\pi f_{max}\cancel{A}\cdot t_{acq} < \frac{\cancel{A}}{2^N-1}$$

$$t_{acq} < \frac{1}{(2^8-1)\cdot 2\pi\cdot 35K}$$

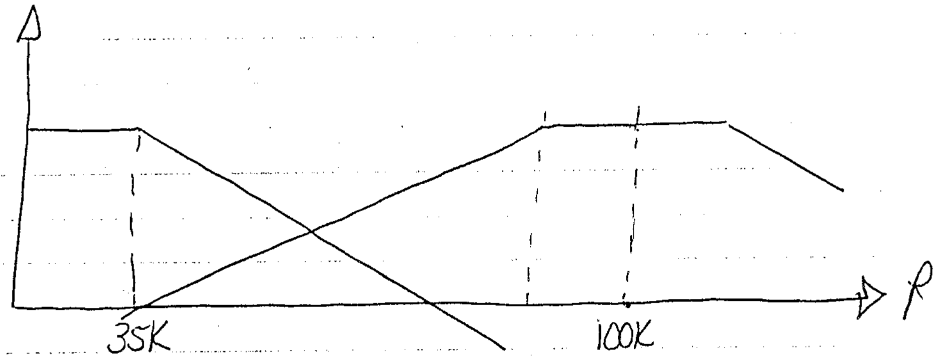
$$t_{acq} < 17.8\ \text{nS}$$ (4)

(ii) ADC sampling freq = 100KHz

i.e 1 sample every 10μs.

Maximum conversion time = 10μs. (2)

(iii)



Above the cut-off frequency, assuming an n^{th} order filter with n identical poles

$$|A_F| = \text{gain} = \frac{1}{(f/f_c)^n} = \left(\frac{f_c}{f}\right)^n$$

$f_c = 35K \quad f = 100 - 35K = 65K$

$\therefore$ Gain of aliased components $= \left(\frac{35K}{65K}\right)^n = (0.538)^n$

Aliased signals must be less than 0.5 LSB

$$2A \cdot (0.538)^n < \frac{A}{2^N - 1}$$

$$0.538^n < 1.96 \times 10^{-3}$$

$$n \log(0.538) < \log(1.96 \times 10^{-3})$$

$$n > \frac{2.9}{2.69} \simeq 10$$

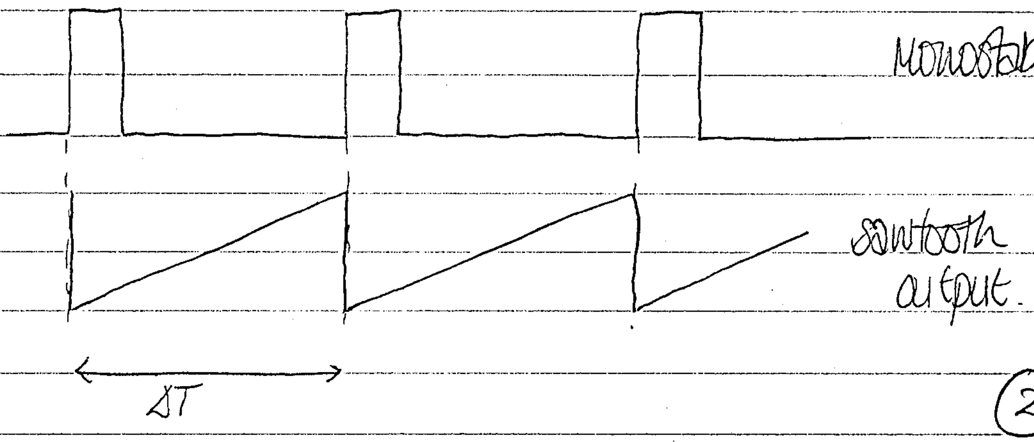
(7)

TOTAL = 25

(4) The input signal is converted to a square wave by the comparator. The rising edge of the comparator output triggers the monostable. Monostable rising edge resets the sawtooth waveform which begins to ramp upwards.

The (maximum) voltage that the sawtooth reaches before being reset depends on the time between monostable pulses, i.e depends on the frequency of the input.

This voltage is sampled by S/H circuit just before the monostable is reset. (3)



(2)

$$V_{max} = 10\,V = \frac{dV}{dt} \cdot \Delta T_{max}$$

$$\Delta T_{max} = \frac{1}{200} = 5mS \quad \therefore \quad \frac{dV}{dt} = 2000\,V/\mu S$$

(2)

A 10-bit ADC is available

$2^{10} = 1024$

$$LSB = \frac{10}{2^{10}-1} = 9.8\text{ mV}$$

The minimum change in period we can detect:

$$\Delta V = \frac{dV}{dt} \cdot \Delta T$$

$$9.8m = 2000\,\Delta T \qquad \Delta T = 4.9\,\mu S$$ 4

(i) At $f = 200\text{ KHz}$, $T = 5\,\mu S$

$V_{out} = 10\text{ mV} \simeq 1\text{ LSB}$

Next 'step' occurs when $V_{out} = 2LSB = 19.6\text{ mV}$

$T = 9.8\,\mu S \qquad f = 102\text{ KHz}$

i.e $\simeq$ 100KHz per step! 3

(ii) At $f = 500\text{ Hz}$, $T = 2\text{ mS}$

$V_{out} = 4\text{ V} = 408\text{ LSB}$

Step above, $V_{OUT} = 409\text{ LSB} = 4.0082\text{ V}$

$\therefore T = 0.0020041$

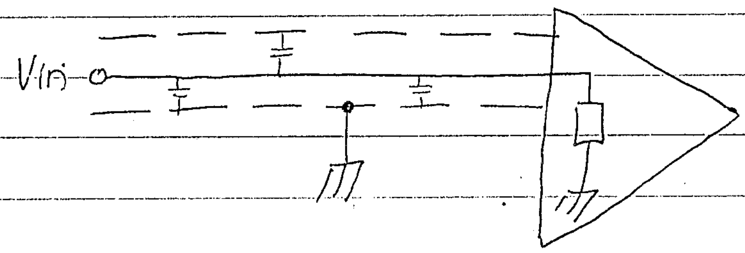
$f = 498.98\text{ Hz}$ 3

Resolution to within $\simeq 1/2\text{ Hz}$

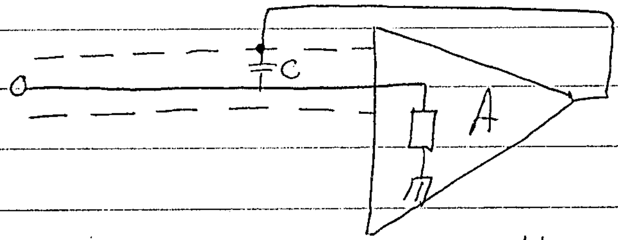
(4). Signals can couple into a circuit via electric or magnetic fields which radiate from any voltage source eg mains.

Balanced circuits reject common-mode signals. Thus external noise / interference which couples eg into power supply, ground, or input leads will appear as a CM signal & will be rejected. (2)

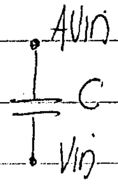
Screened cable can be used to shield input terminals from interference. However this can add significant capacitance to the input terminals. (2)



A solution is to use a guard shield:



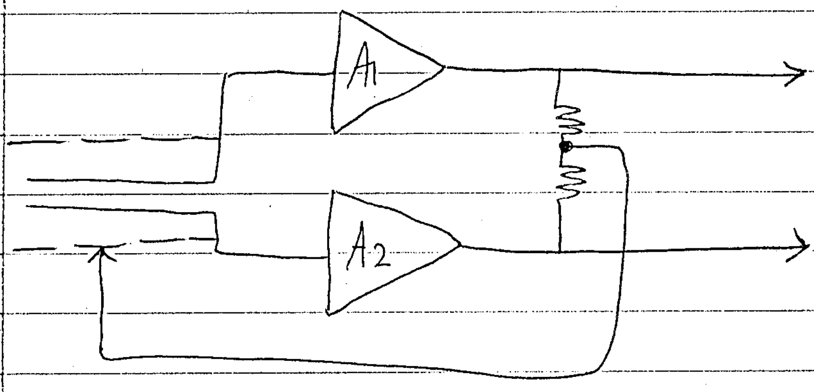
effective capacitance:



$$i_c = sC(V_{in} - AV_{in}) = sC(1-A)V_{in}$$

ie $C_{effective}$ reduced if $A \simeq 1$ (2)

Balanced guard Shielding:



2

TOTAL = 25

Q5.

(a) $V_{out} = V_{be}(1 + R_2/R_1) - I_{ref} \cdot R_2$

$V_{be} = V_{be}(27) + T_c(T-27)$

$\therefore V_{out} = V_{be}(27)[1 + R_2/R_1] + T_c(1+R_2/R_1)(T-27) - I_{ref} \cdot R_2$ (2)

$\frac{\partial V_{out}}{\partial T} = T_c(1+R_2/R_1)$

$T_c = \partial V_{be}/\partial T = -2.1 \times 10^{-3}\ V/°C$

Require $\partial V_{out}/\partial T = 0.1\ V/°C \quad \therefore 1+R_2/R_1 = 47.6$

At 0°C:

$V_{out} = V_{be}(27)(1+R_2/R_1) + T_c(1+R_2/R_1)(-27) - I_{ref} \cdot R_2$

$= 0.68 \times 47.6 - (2.1 \times 10^{-3})(47.6)(-27) - I_{ref} R_2$

$= 32.36 + 2.7 - I_{ref} \cdot R_2$

$= 0$

$\therefore R_2 = 35.06/I_{ref} = 35.06 K\Omega$ (if I_{ref} = 1mA) (2)

$\Rightarrow R_1 = 752\Omega$ (2)

I_{ref} in practice 0.9 – 1.1 mA

$V_{out} = 35.06 - I_{ref} \cdot (35.06K)$ at 0°C

@ 0.9 mA : $V_{out}(0°) = 3.5V$

@ 1.1 mA : $V_{out}(0°) = -3.5V$.

At 0.9mA require $R_2 = 38.95 K\Omega$ (assuming R_2/R_1 is fixed)

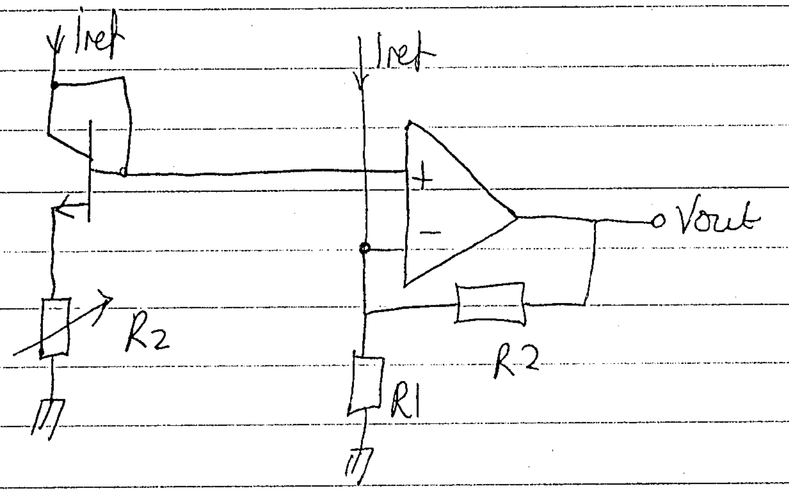
At 1.1mA require $R_2 = 31.87 K\Omega$ (" " ")

Thus R_2 31.87 → 38.95 KΩ

R_1 683 → 836 Ω

Tuning range. (6)

Nulling Vout using a single resistor:



$$V_{out} = V_{be}(1+R2/R1) - I_{ref}R_2 + I_{ref}R_Z(1+R_2/R_1).$$

Vout can be nulled by varying R_Z. 3

Suppose we have a noisy sinusoid:

$$V_s \cos\omega_s t + n(t)$$

We cross-correlate this with a signal of the same frequency:

$$V_r \cos(\omega_s t + \phi)$$

$$R_{xy}(\tau) = \frac{1}{T}\int_0^T \left[V_s \cos\omega_s(t-\tau) + n(t-\tau)\right] V_r \cos(\omega_s t + \phi)\, dt$$

The cross-correlation of the reference V_r with noise $n(t)$ will be zero provided the integration time t is long. Thus the resulting output:

$$R_{xy}(\tau) = \frac{1}{T}\int_0^T V_s V_r \cos\omega_s(t-\tau) \cdot \cos(\omega_s t + \phi)\, dt$$

$$= \frac{V_s V_r}{2} \cos(\omega\tau + \phi)$$

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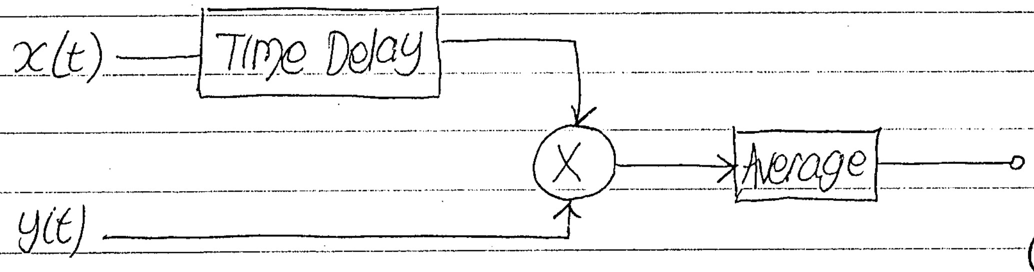
We adjust τ until $R_{xy}(\tau)$ is a maximum. This also gives phase information. (3)

Block diagram:



(2)

If the signal frequency is not known we multiply the signal with a time-delayed version of itself (auto-correlation)

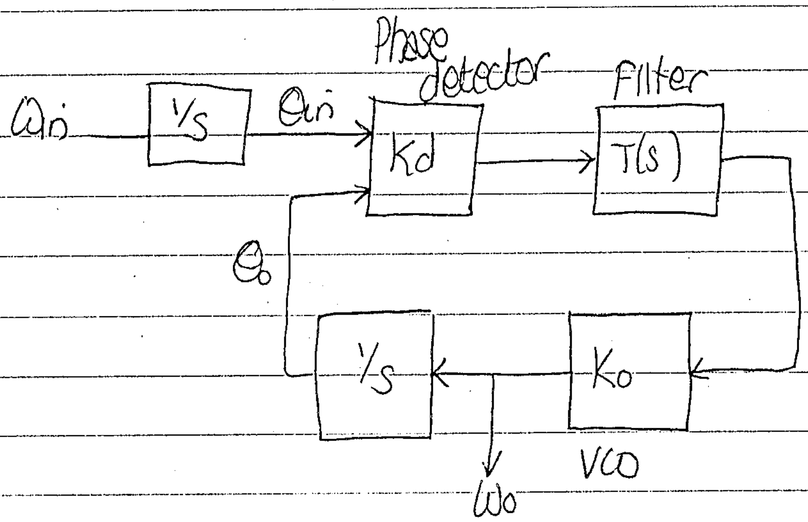
$$R_{xy}(\tau) = \frac{1}{T}\int_0^T \left[V_s \cos\omega_s(t-\tau) + n(t-\tau)\right]\left[V_s \cos\omega_s t + n(t)\right] \cdot dt$$

Cross correlation function between signal & noise will be zero. The autocorrelation function of the signal will be superimposed on that of the noise, & will be periodic. Hence signal period can be determined for subsequent cross-correlation

(5)

TOTAL = 25

(6)



$$LG = \frac{K_d K_o T(s)}{s}$$

Closed loop gain, $\frac{\omega_o(s)}{\omega_{in}(s)} = \frac{K_d K_o T(s)}{s + K_d K_o T(s)}$

$$T(s) = \frac{1}{1 + s/\omega_p}$$

$$\therefore \frac{\omega_o(s)}{\omega_{in}(s)} = \frac{K_d K_o \omega_p}{s^2 + s\omega_p + K_d K_o \omega_p}$$ (3)

$2f_L = 350\,KHz \quad \therefore \quad R_1 C_1 = 2 \times 10^{-5}$. (1)

$f_{OFFSET} = 250\,KHz$:

$R_2 = 300K, \quad C_1 = 150pF \quad \Rightarrow R_1 = 133K\Omega$

or $R_2 = 150K, \quad C_1 = 250pF \quad \Rightarrow R_1 = 80K$

or $R_2 = 10K, \quad C_1 = 3.5nF \quad \Rightarrow R_1 = 5.71K$

or $R_2 = 3K, \quad C_1 = 20nF \quad \Rightarrow R_1 = 1K$

(3)

$S^2 + S\omega_p + K_oK_d\omega_p$

$\Rightarrow S^2 + S(\zeta\omega_n) + \omega_n^2$

$\omega_n^2 = K_oK_d\omega_p \qquad \zeta = \sqrt{\omega_p/K_oK_d}$

$K_o = 4\pi f_c / V_{cc} = 4.40 \times 10^3 \ rV^{-1}$

$K_d = \frac{V_{cc}}{\pi} = 1.59$

$[100 \cdot 10^3]^2 = 1.59 \cdot 440 \times 10^3 \ \omega_p$

$\omega_p = 14.3\,K \ rs^{-1}$ (2)

$f_p = 2.27 \ KHz$

$\zeta = 0.14$ (2)

OR: IF THEY TAKE

$\omega_n^2 = [2\pi \cdot 100 \cdot 10^3]^2$

$\omega_p = 564.3 \ K\,r/s$

$\zeta = 0.9$

Lightly damped ∴ likely to lose lock if input is very noisy. (1)

Capture range is wide, as the filter bandwidth is wide (1)

Wide filter bandwidth will give less attenuation of PD output signal, ie modulation of VCO output

Filter gain $= \frac{1}{1 + jf/f_p} \simeq \frac{f_p}{f}$ if $f \gg f_p$

eg if $f = 500KHz$ (minimum), $\frac{f_p}{f} \simeq 0.0045$

$0.0045 \times 5 = 0.02V$ ripple! (4)

(OR : 0.9V IF THEY USE $f_p = 89.8KHz$!)

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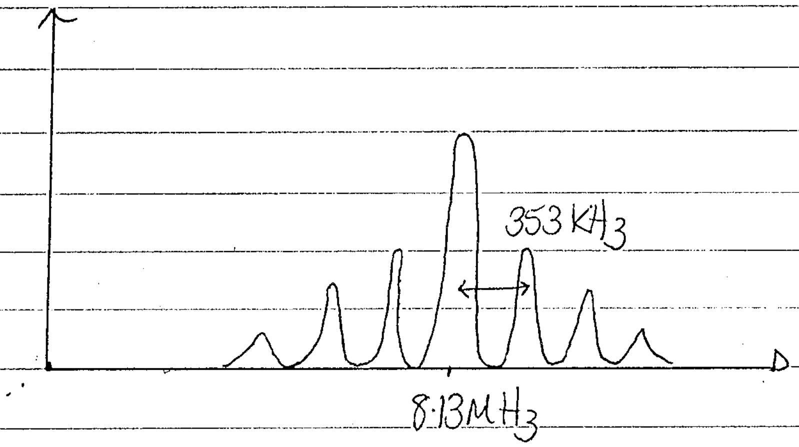
Fractional N synthesiser:

Average divide ratio = $\frac{20\times8 + 3\times9}{23} = 8.13$

$\therefore$ Average VCO output frequency = 8.13MHz (4)

The fractional-N sidebands will be spaced at (multiples of) the modulation frequency, which is 23 cycles of the VCO output, ie at $f_m = 353.5$kHz

VCO output spectrum:



(4)

TOTAL = 25.