Paper Number(s): **E3.01**
AC1

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2000

MSc and EEE PART III/IV: M.Eng., B.Eng. and ACGI

ANALOGUE INTEGRATED CIRCUITS AND SYSTEMS

Monday, May 8 2000, 10:00 am

There are SIX questions on this paper.

Answer FOUR questions.

All questions carry equal marks.

Time allowed: 3:00 hours

Corrected Copy
Q1

Examiners: Prof C. Toumazou, Dr A.J. Payne

Special instructions for invigilators: None

Information for candidates: None

1. Voltage and current-sources are key components in analogue circuit design. Sketch a typical band-gap voltage reference circuit and prove that the temperature coefficient of the output voltage V_0 is zero if $V_0 = 1.283$ V.
Assume the temperature coefficient of V_{BE} to be -2.5mV/°C, Boltzmanns constant $k = 1.38 \times 10^{-23}$ J/K and electron charge $q = 1.6 \times 10^{-19}$ C.
Assume a value of V_{BE}. [11]

Calculate the fractional temperature coefficient for the constant current generator of *Figure 1(a)* at room temperature, given that R is a polysilicon resistor with a temperature coefficient of 1500 ppm/°C. [7]

Explain qualitatively why the four-transistor voltage potential divider of *Figure 1(b)* can have significantly less active-chip area than an equivalent two-transistor voltage potential divider with the same power consumption. [7]

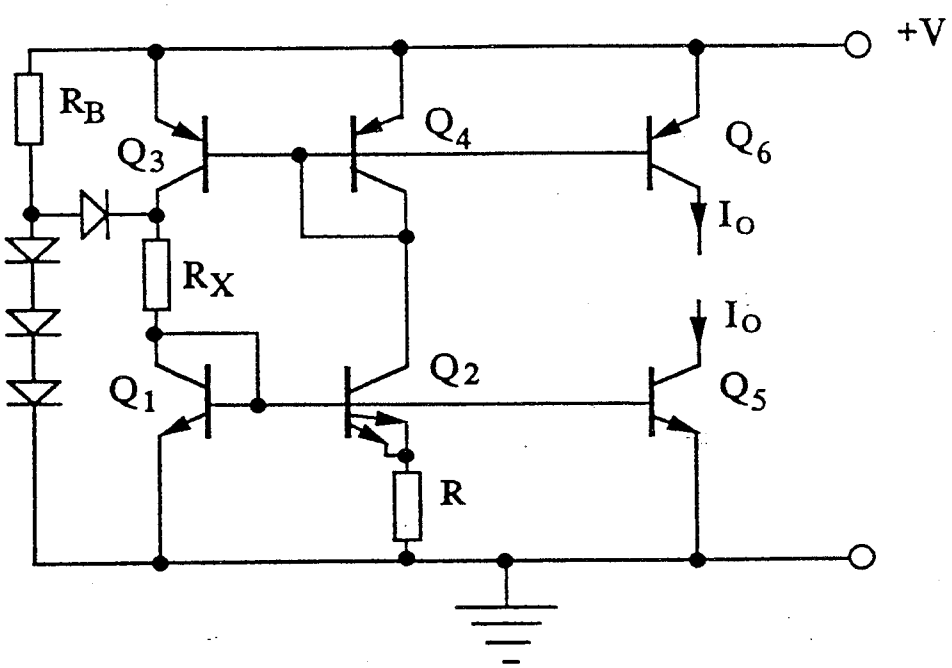

Figure 1(a)

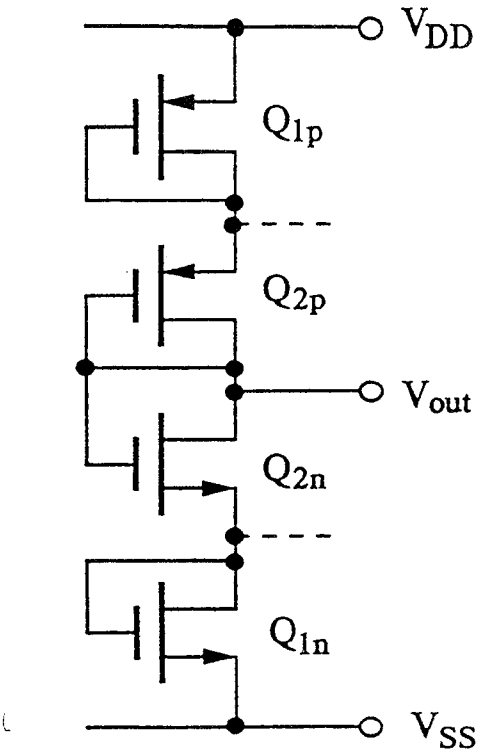

Figure 1(b)

2. Sketch typical circuit diagrams for a two-stage cascoded and a single-stage CMOS op-amp. Explain why the single-stage design has potentially much higher bandwidth than the two-stage design and in particular why it is not necessary to Miller compensate the single-stage architecture. Give one advantage and one disadvantage of the cascoded op-amp. [10]

Estimate the low-frequency differential voltage gain, slew rate, gain-bandwidth product and maximum positive output swing of the two-stage CMOS op-amp shown in *Figure 2*. Aspect ratios of all devices are shown on the circuit. Assume all bulk effects are negligible. Device model parameters are given below. [12]

Explain qualitatively why the addition of a load capacitor to the output of a two-stage op-amp degrades amplifier stability, whereas an additional load capacitor connected to the output of a single-stage op-amp improves amplifier stability. [3]

CMOS TRANSISTOR PARAMETERS

MODEL PARAMETERS	Kp ($\mu A/V^2$)	λ (V^{-1})	V_{To} (V)
PMOS	20	0.03	- 0.8
NMOS	30	0.02	1.0

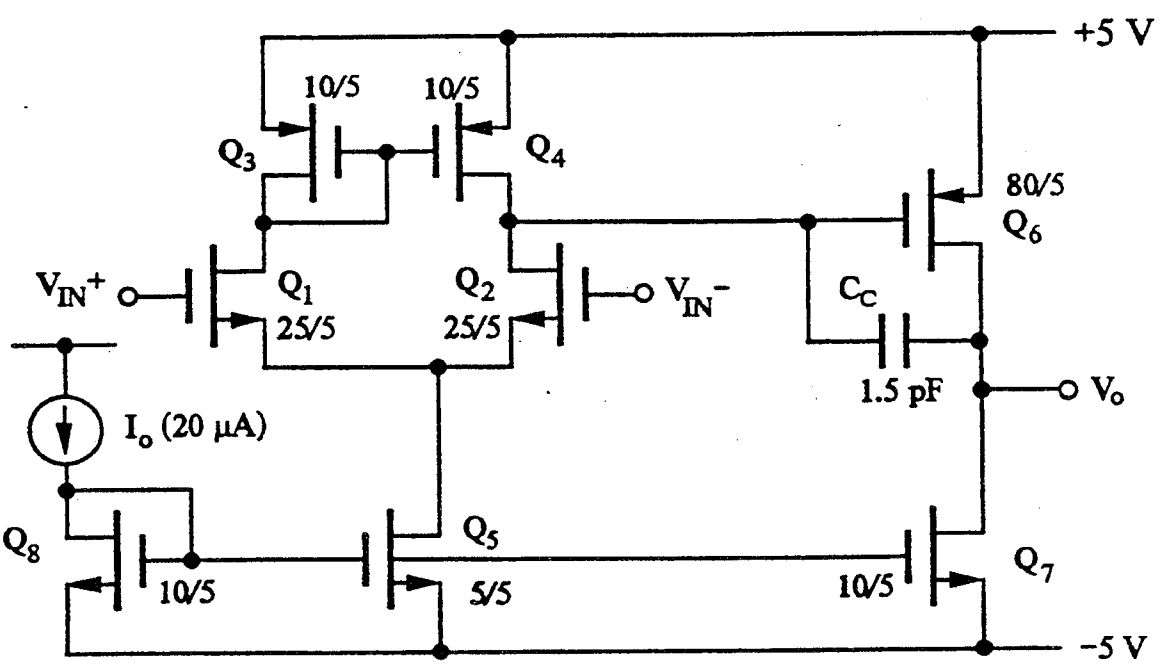

Figure 2

3. Under what operating conditions does the MOSFET of *Figure 3*(a) realise a linear floating resistor between terminals A and B ? Show that under these conditions the equivalent resistance R_{AB} can be approximated by

$$R_{AB} = \frac{L}{KW(V_{GS} - V_T)}$$

stating any assumptions. All symbols have their usual meaning. [6]

Discuss three sources of non-linearity in the single MOSFET resistor realisation of *Figure 3(a)* and suggest one suitable circuit design to help eliminate one or more of these non-linear terms. Show all necessary circuit analysis to confirm your design. [6]

Figure 3(b) shows a fully differential continuous time integrator using a balanced double differential linear active transresistor. Derive an expression for the time constant of the integrator. You may ignore all bulk effects, and assume all MOSFETs are operating in the triode region. [8]

Finally, for the current mirror of *Figure 3*(c) estimate the minimum output voltage while still maintaining saturated devices. Derive this voltage swing in terms of device threshold voltage V_T, clearly stating any assumptions you make. [5]

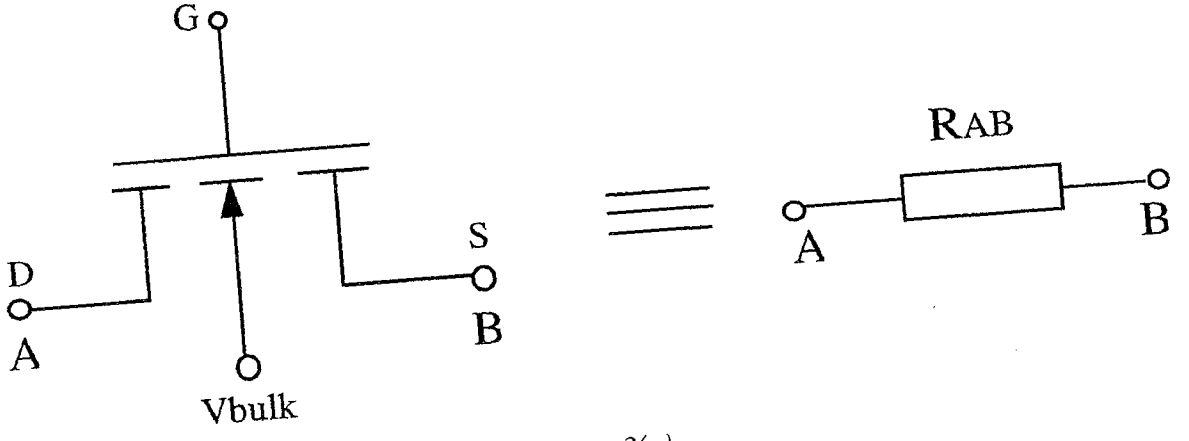

Figure 3(a)

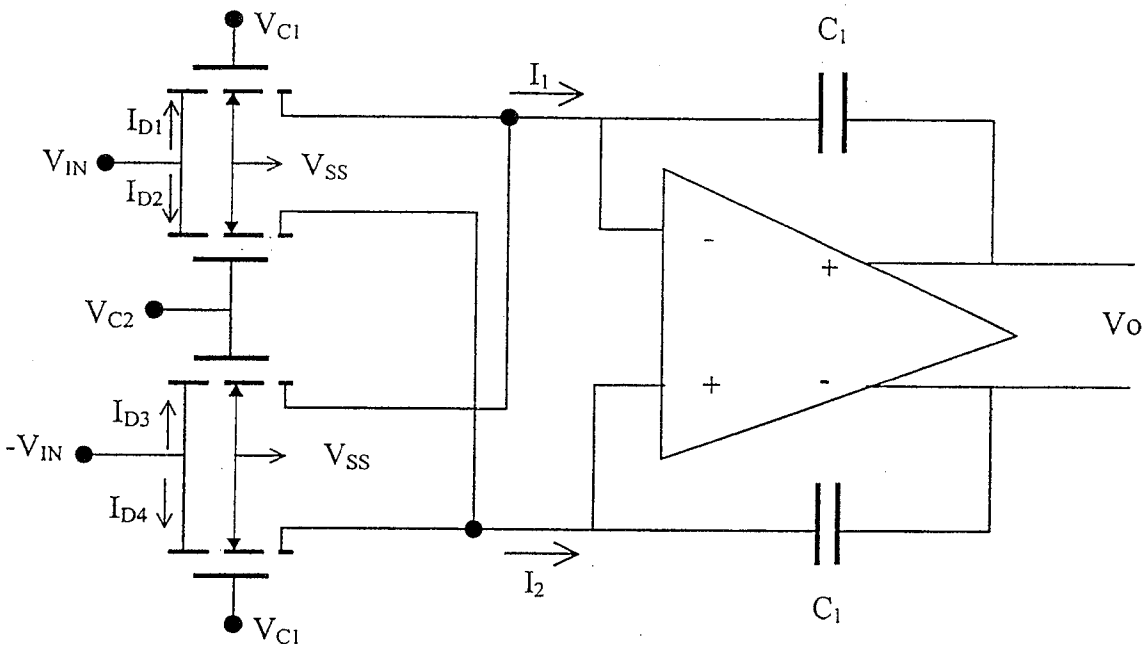

Figure 3(b)

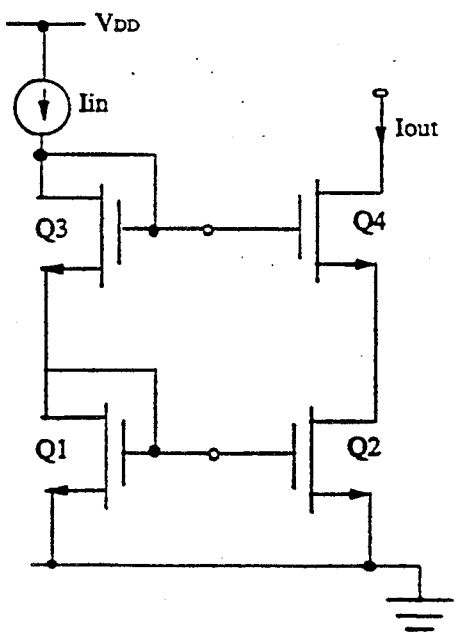

Figure 3(c)

4. Very high frequency single chip integrated filters make use of the linear transconductance based integrator of *Figure 4 (a)* Show how two of these transconductors can be connected to simulate the impedance of a small value inductor, and derive an expression for the inductance. [8]

Figure 4(b) shows a simplified diagram of the core section of a fully differential folded cascode operational amplifier with a common-mode feedback block. Sketch a suitable common-mode feedback circuit. What is the main advantage of a folded cascode amplifier compared to a classical cascode connection ? [7]

Finally, a sampled-data methodology which overcomes amplitude accuracy constraints encountered with the previous continuous-time circuits is the oversampling technique. Briefly explain the principle of oversampling or sigma-delta modulation. Sketch a typical architecture for an analogue to digital converter based upon this method, explain its principles of operation, in particular the feedback noise shaping mechanism. [10]

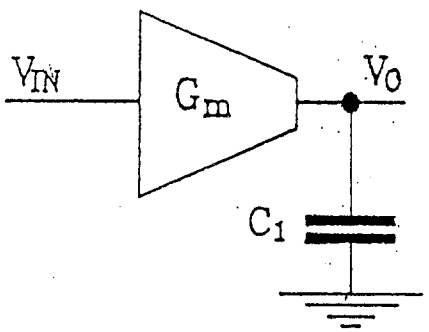

Figure 4(a)

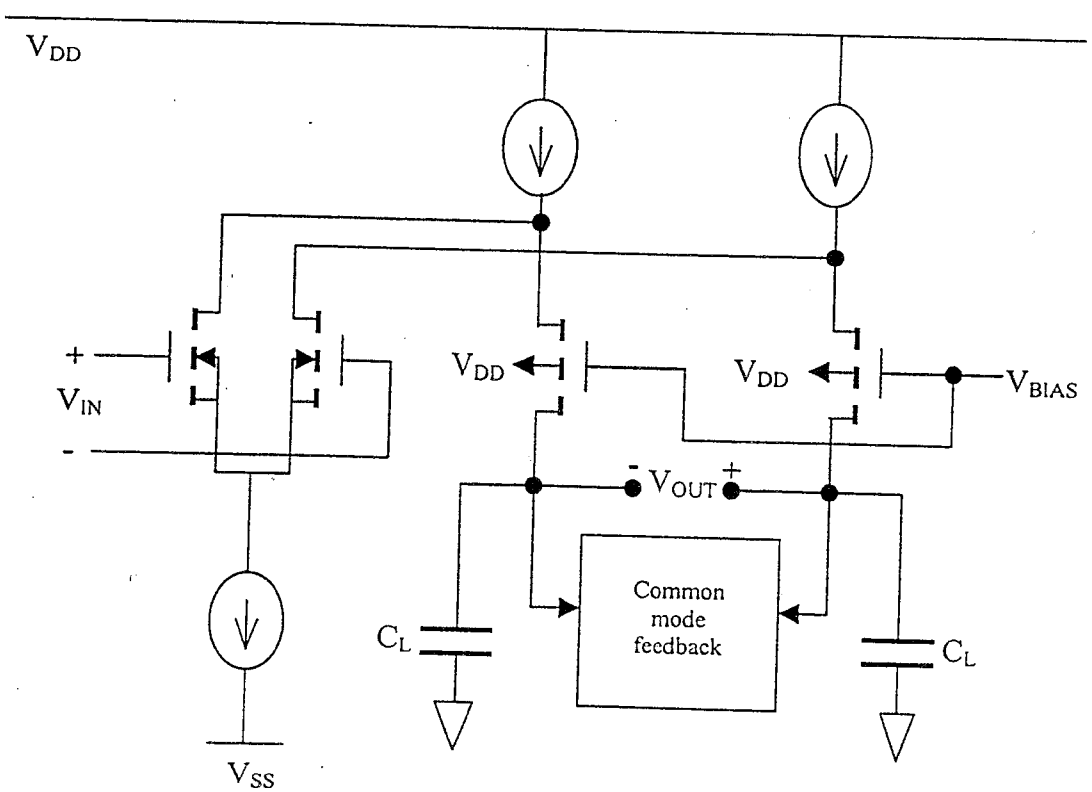

Figure 4(b)

5. Briefly discuss the following with respect to high frequency circuits:
   Decoupling capacitors;
   50 ohm termination;
   BNC connector;
   Ground plane. [8]

The circuit shown in *Figure 5* is a single bit cell of a current-mode algorithmic analogue to digital converter. Briefly describe the operation of the cell and give reasons why this converter is particularly suited to mixed analogue and digital VLSI. [9]

Assuming that the maximum resolution of any sampled-data converter is limited by switch noise (kT/C), calculate the maximum resolution of a stereo-audio system running at a sample rate of 40 kHz. Assume a MOSFET switch aspect ratio (W/L) = 1/8, transconductance parameter $K = 20\ \mu A/V^2$ and a device threshold voltage $V_T = 1$ V.
The *on* voltage of the switch is a 5 V reference (i.e. $V_{GSon} = V_{ref} = 5$ V). You may also assume that the switch settles in $10\ \tau$ (where τ = time constant) over one period of the clock frequency. [8]

Boltzmanns constant $k = 1.38 \times 10^{-23}$ J/K and the ambient temperature is 300 K.

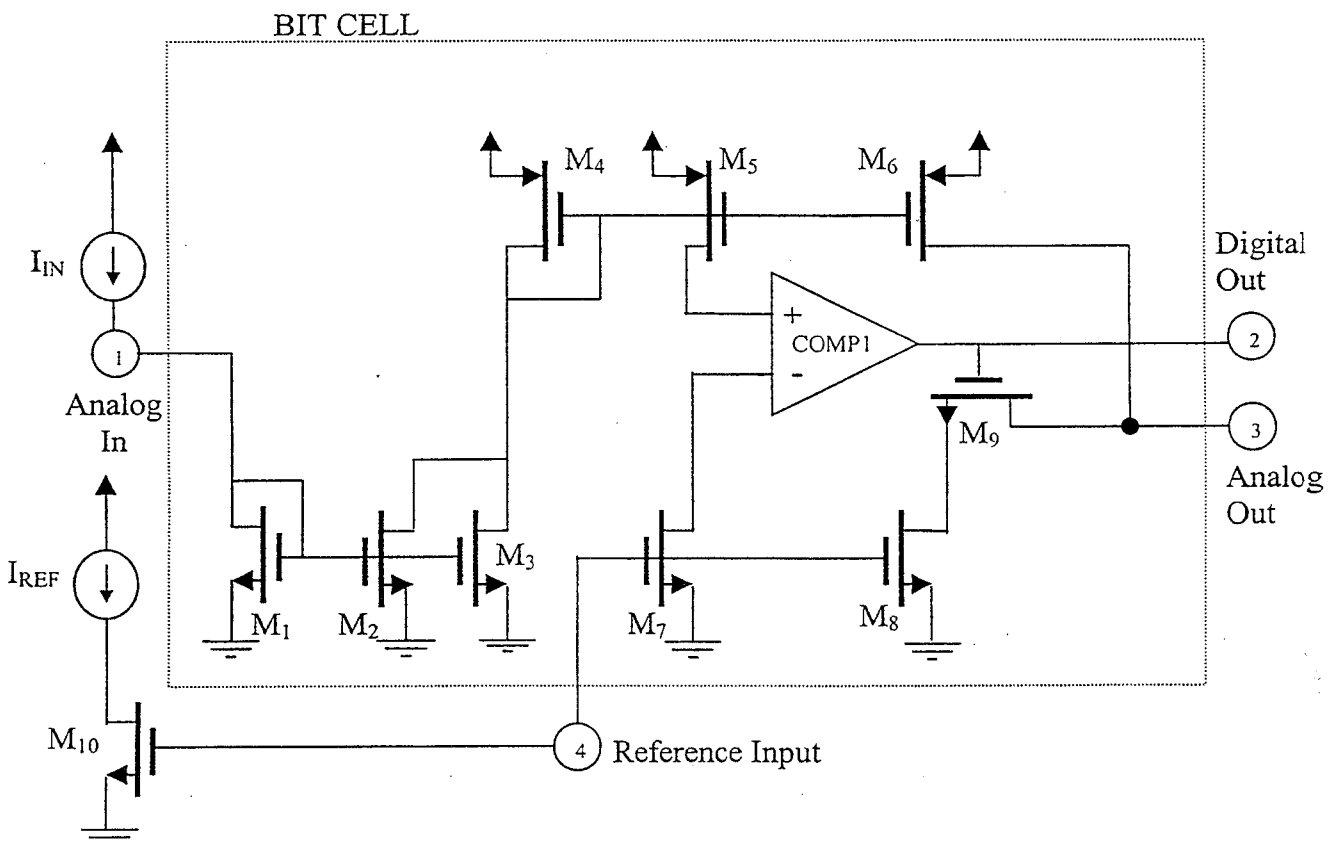

Figure 5

6. Give one advantage and one disadvantage of integrated continuous-time filters compared with discrete-time sampled-data filters. [2]

Figure 6 shows three sampled-data integrator building blocks. Derive an expression for the transfer function of the integrators of *Figure 6(a)* and *Figure 6(b)*. All switches are implemented by MOSFETs of equal size. Assume that the integrators are driven by non-overlapping clocks with a clock frequency much higher than the maximum input signal frequency. Also assume the switches are ideal.

[12]

Figure 6(c) shows one section of a switched-capacitor ladder filter. Based on this filter structure design a 3rd-order Chebyshev low-pass switched-capacitor filter with a cut-off frequency of 5 kHz and a 1.0 dB pass-band ripple. Assume a clocking frequency of 100 kHz. Passive component values for the L-C prototype, normalised to 1 rad/s, are $C_1 = C_3 = 2.0236$, $L_2 = 0.994$. In your analysis you may assume all integrators to be lossless. [11]

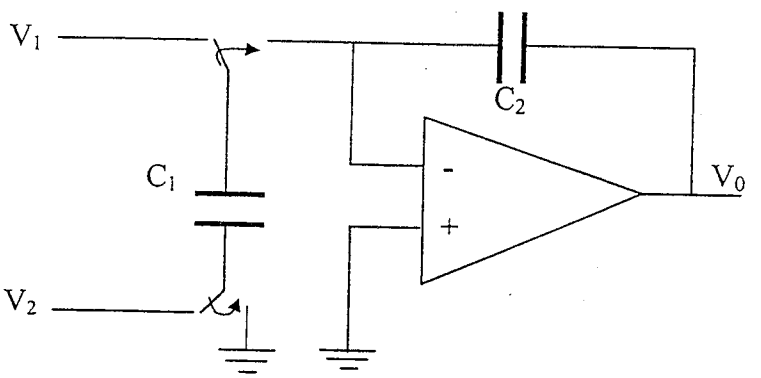

Figure 6(a)

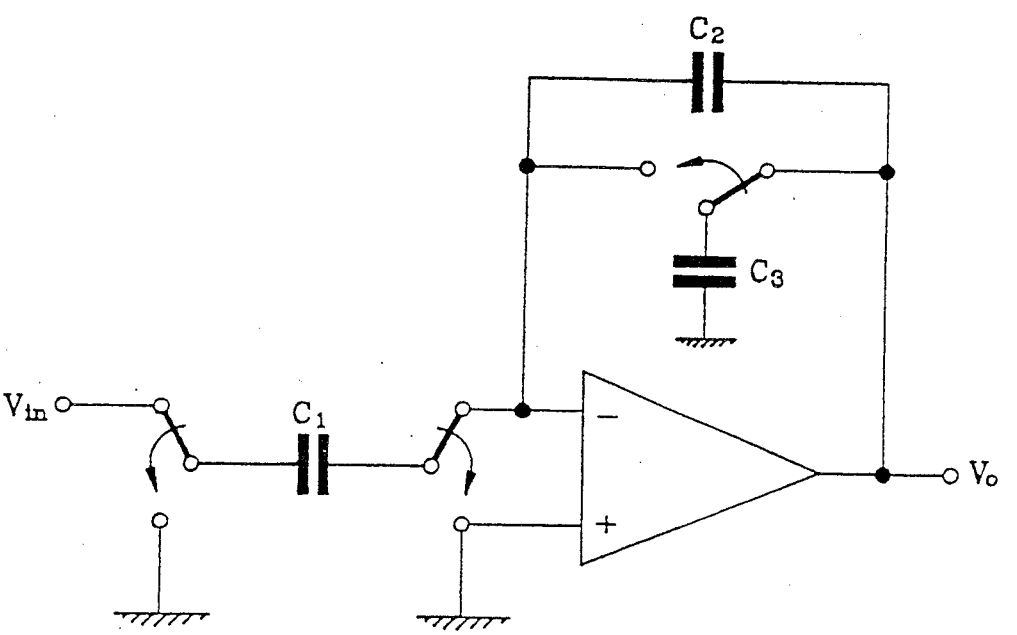

Figure 6(b)

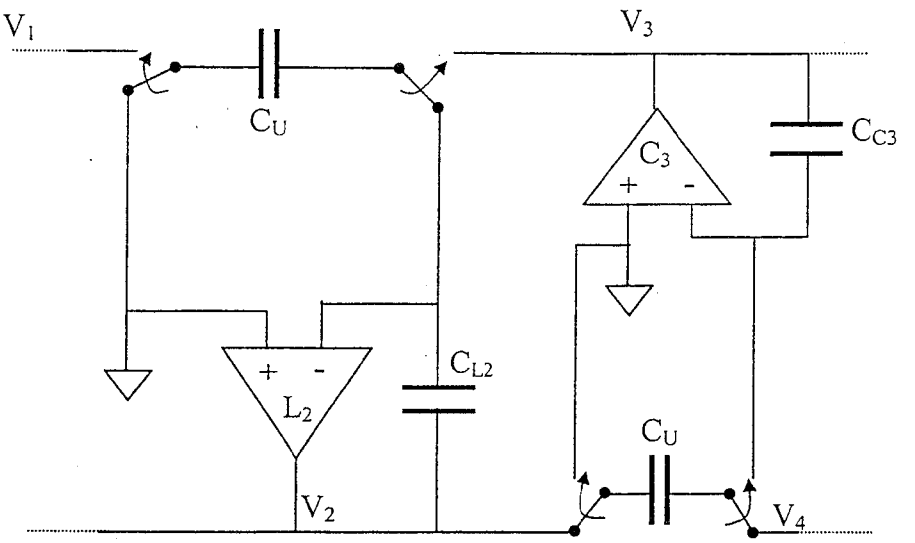

Figure 6(c)

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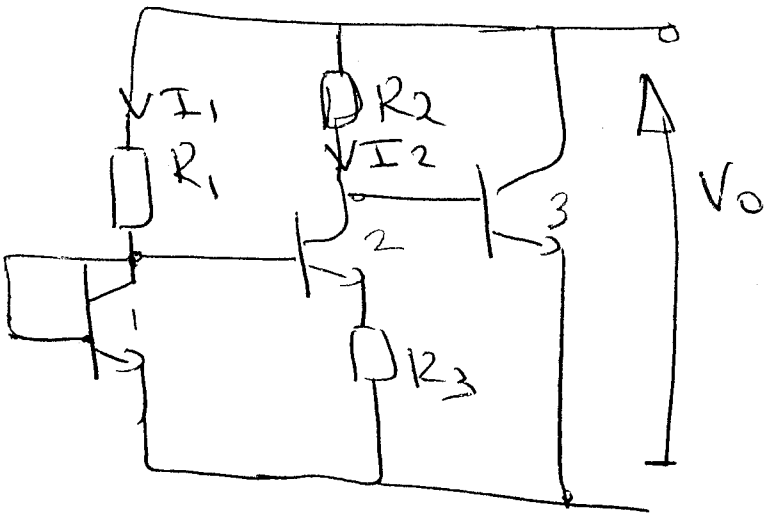
EXAM SOLUTIONS

C. TOUMAZOU.

Q1.



Bandgap.

5/5

$$V_{BE1} = V_{BE2} + I_2 R_3$$

$$\beta >> 1$$

Since $V_{BE1} - V_{BE2} = V_T \ln(I_1/I_2)$

Then $V_o = V_{BE3} + R_2/R_3 \, V_T \ln(I_1/I_2)$

$V_T \ln(I_3/I_S)$ → assume Non-temp

for $dV_o/dt = 0$, then dV_{BE3}/dT

$$= \frac{V_T}{T} \frac{R_2}{R_3} \ln\left(\frac{I_1}{I_2}\right)$$

Since $\frac{dV_{BE}}{dt} = -2.5\,mV/°C$, $\frac{V_T}{T} = \frac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}}$

Then $\left(\frac{R_2}{R_3}\right) \ln\left(\frac{I_1}{I_2}\right) = 29$ and so

6/6

$$V_o = 1.283\,V$$

//

For PTAT temperature coefficient of V_T cancels with negative temp coefficient of Resistor

1 cont

$\therefore T_{CF} = \frac{1}{V_T} \partial V_T/\partial T - 1/R \, \partial R/\partial T$

(7/7) $= 1/T - 1500 \times 10^{-6}$ @ RoomT $= 1833$ ppm/°C

Figure 1(c).

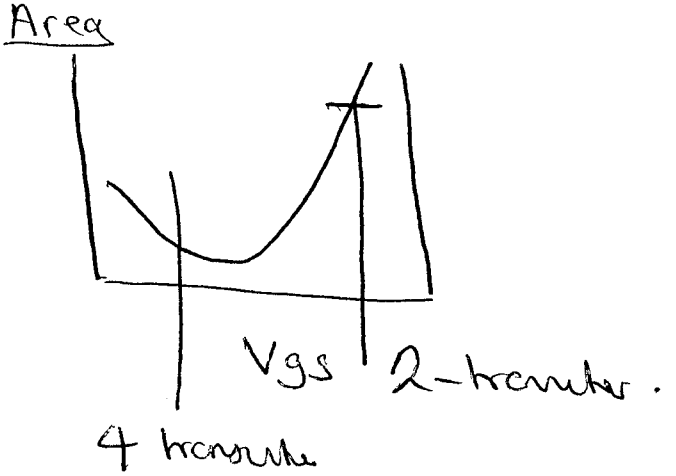
Since $I = \frac{kW}{2L} (V_{SS} - V_T)^2$

then if V_{gs} is small $\simeq V_T$
then (W/L) large.

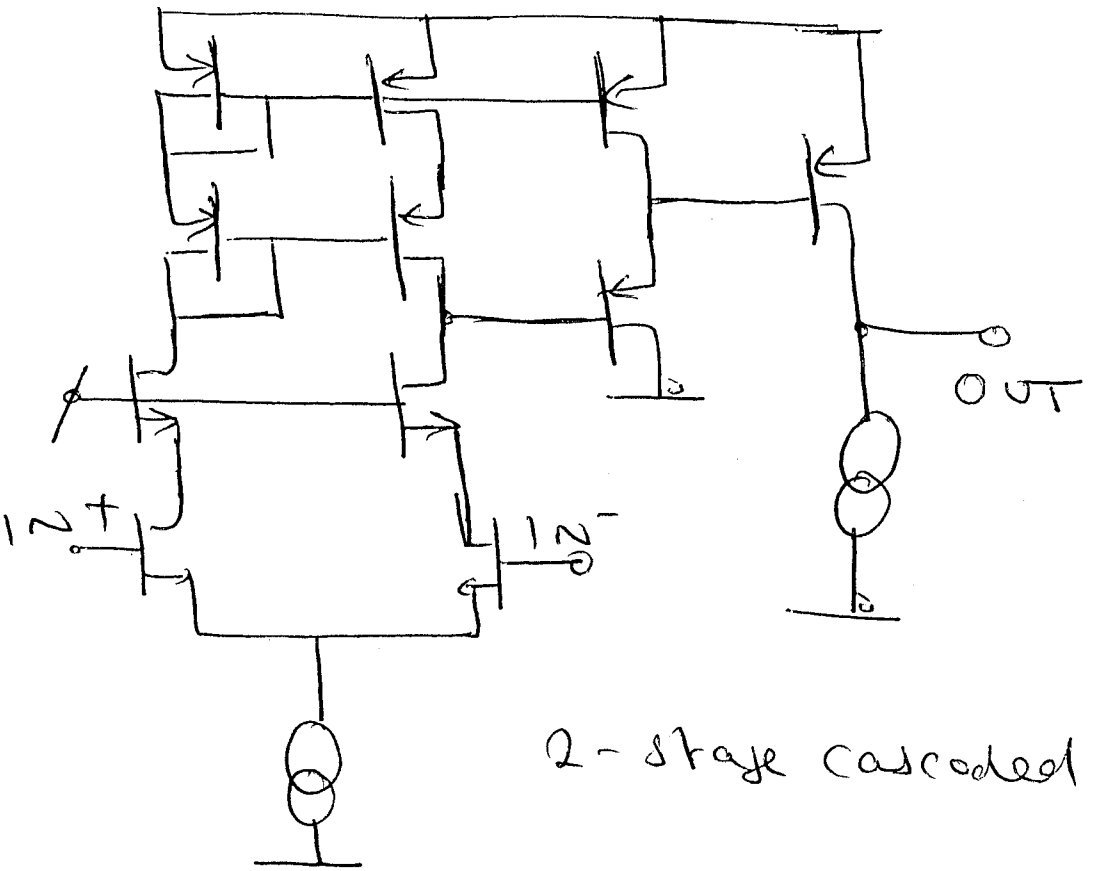
If $V_{SS} >> V_T$
then (W/L) small
Small (W/L) gives large chip area

∴ Two transistor P.D
has larger V_{SS} / transistor
than four transistor P.D for same
supply.

(7/7)

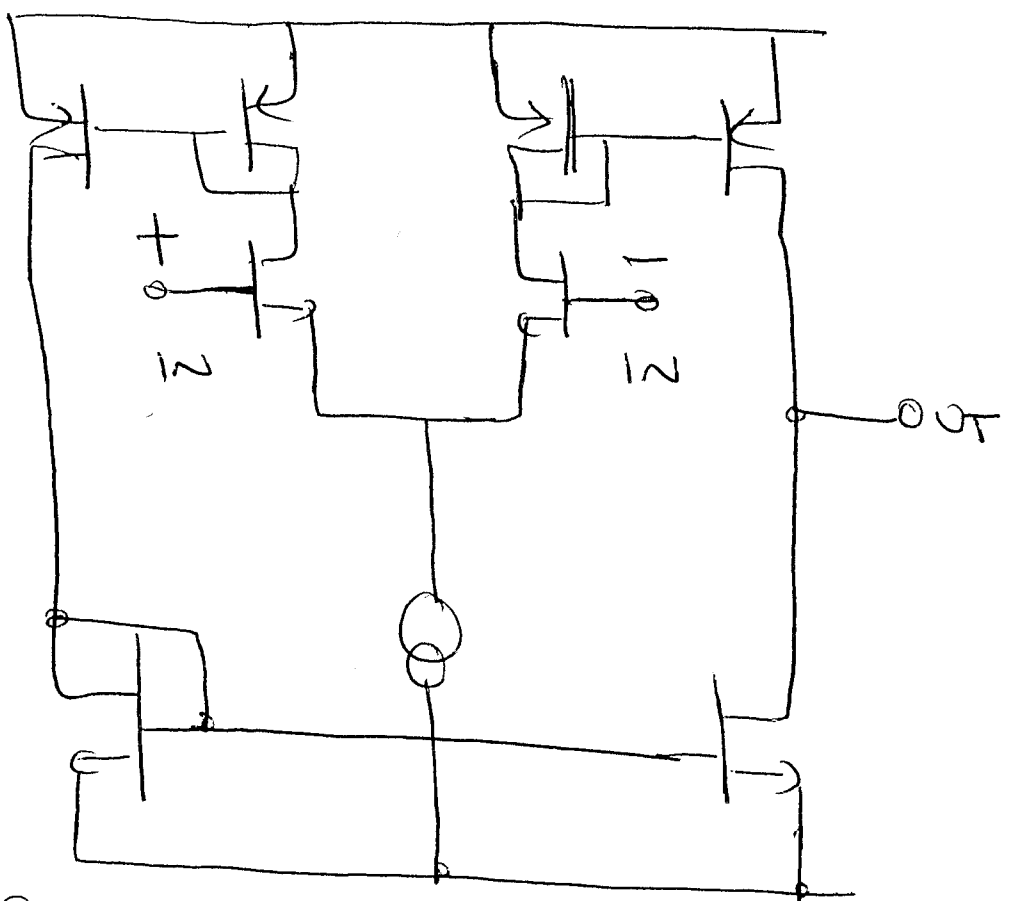


Q2.



3/3

2-stage cascoded.



3/3

Single-stage.

Q2 (Cont)

In a single-stage the main high impedance node is at the output. Compensation is then provided via a load capacitance at the output. The internal poles at the lower impedance nodes are now secondary and will only affect the phase margin of the amplifier.

In a two-stage design, the requirement for a single high internal impedance to achieve voltage gain means that the amplifier requires internal frequency (miller) compensation to be stable. Because of this compensation the bandwidth is reduced.

The main advantage of a cascoded op-amp is voltage gain, the main disadvantage is CMVR or signal swing limitations. 4/4

Op-Amp

2/2 $A_{V1} = -g_{m2}/(g_{O2}+g_{O4})$

$(g_{O2}+g_{O4}) = I_{D2}(\lambda_n + \lambda_p) =$

$5\times10^{-6}\times0.05 = 2.5\times10^{-7}\ \Omega^{-1}$

2/2 $g_{m2} = 2\sqrt{\beta_2 I_D} \Rightarrow \beta_2 = \frac{k_N}{2}\left(\frac{W}{L}\right)_2 = 7.5\times10^{-5}\ A/V$

$g_{m2} = 3.87\times10^{-5}\ S$, $A_1 = -154.9$

$A_2 = -g_{m6}/(g_{O7}+g_{O6})$

Q2-Cont.

$$(g_{06}+g_{07}) = I_{D6}(\lambda_{NP}+\lambda_N) = 20\times10^{-6}\times0.05$$
$$= 10\times10^{-7}\ \Omega^{-1}$$

(2/2) $$g_{m6} = 2\sqrt{\beta_6 I_{D6}} \Rightarrow \beta_6 = \frac{k_p}{2}\left(\frac{W}{L}\right)_6 = 1.6\times10^{-4}\ A/V^2$$

$$g_{m6} = 1.13\times10^{-4},\ A_2 = 113$$

$$A_{TOTAL} = A_1 A_2 = 17503$$

(2/2) $$G.B_p = g_{m2}/2\pi C_c = 4.1\ MHz$$

(1/2) $$S.R = I_o/C_c = \left(\frac{10}{1.5}\right) V/\mu s$$

MAXIMUM SWING

$$[5V - V_{SD(6)}] \Rightarrow [5 - (V_{SG} - V_T)]$$

For Schematic.

Assume $V_{SG6} = V_{DS4} = V_{SG3}$

$$V_{SG3} = \left(V_{T(3)} + \sqrt{\frac{I_o}{4\beta_3}}\right)$$

(2/2) $$\beta_3 = \left(\frac{kW}{2L}\right)_3 \Rightarrow$$ maximum swing =

In 2-stage load is 2nd pole hence reducing load increases bandwidth.

(3/3) With single-stage load come dominant pole hence reducing load increases bandwidth.

Q3 Assumption is that if $(V_{DS} \approx 0)$ or $(V_{DS} << (V_{GS} - V_T)$ device acts in linear region. From

$$I_D = \frac{KW}{L}\left[(V_{GS} - V_T)V_{DS} - V_{DS}^2/2\right](1 + \lambda V_{DS})$$

for $V_{DS} << (V_{GS} - V_T)$, then $\lambda V_{DS} << 1$

So $$I_D = \frac{KW}{L}(V_{GS} - V_T)V_{DS}$$

6/6

OR $$R_{AB} = V_{DS}/I_D = L/(KW(V_{SS} - V_T)$$

Three sources of Non-linearity

(i) Limited due to V_{BS} changing V_T for resistive V_{DS} due to body effect. ie $V_T = V_{TO} + \gamma\left[\sqrt{-V_{BS} + 2\phi_F} - \sqrt{2\phi_F}\right]$

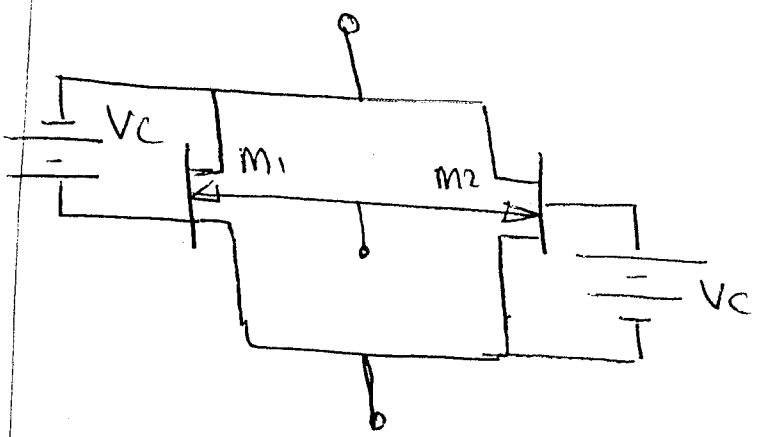
γ = bulk threshold parameter

ϕ_F = Fermi-level potential

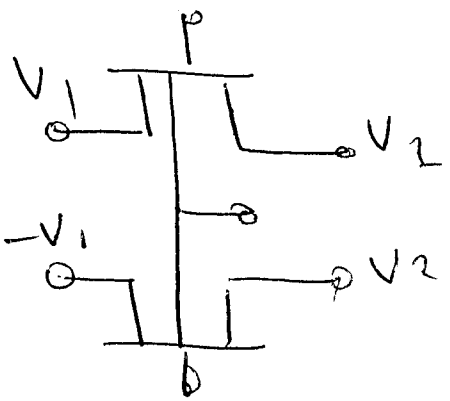
(ii) Limited due to V_{DS} approaching $(V_{GS} - V_T)$ hence saturation region for large positive V_{DS}.

(iii) For large values of V_{DS} the $V_{DS}^2/2$ term comes in making the resistor quite non-linear.

4/4

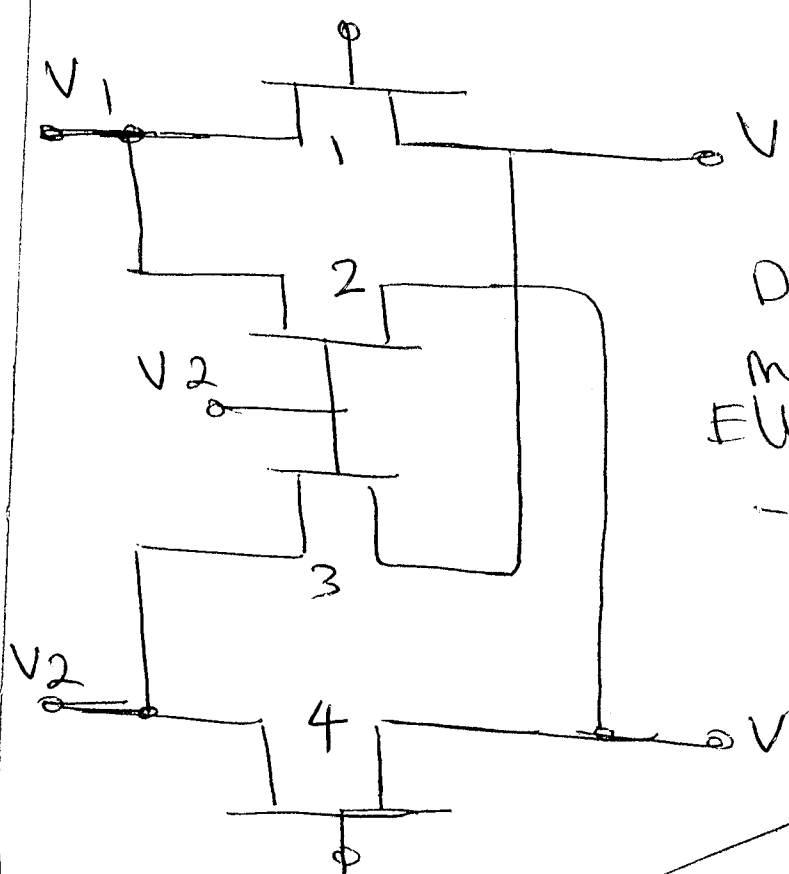


Parallel circuit – eliminates $V_{ds}^2/2$ term.



Differential scheme

Effects of Vos cancelled.



Double differential MOS.

Eliminates
- Vos and V_T term.

ANY one of these will do!

2/2

Double differential integrator

$$I_{D1} = 2\beta\left[(V_{C1} - V - V_T)(V_1 - V) - \tfrac{1}{2}(V_1 - V)^2\right]$$

$$I_{D2} = 2\beta\left[(V_{C2} - V - V_T)(V_1 - V) - \tfrac{1}{2}(V_1 - V)^2\right]$$

$$I_{D3} = 2\beta\left[(V_{C2} - V - V_T)(V_2 - V) - \tfrac{1}{2}(V_2 - V)^2\right]$$

$$I_{D4} = 2\beta\left[(V_{C1} - V - V_T)(V_2 - V) - \tfrac{1}{2}(V_2 - V)^2\right]$$

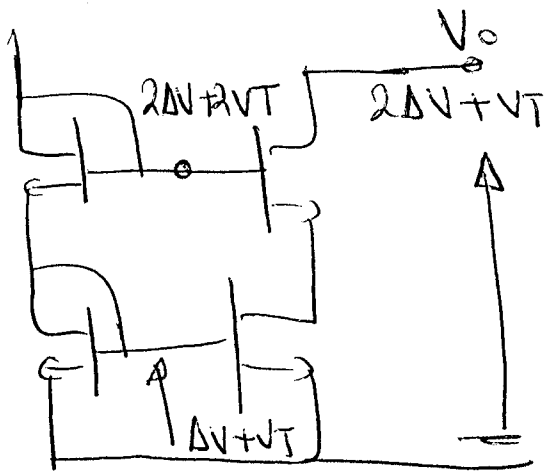
Expanding it can be shown that :-

$$(V_1 - V_2)/(I_1 - I_2) = 1/2\beta(V_{C1} - V_{C2}) = R$$

Independent of both V_T and V_{DS} terms

Hence $\tau = 2CR = \dfrac{C}{\beta(V_{C1} - V_{C2})}$

8/8



5/5

Assume $\Delta V = V_{GS} - V_T$

for sat

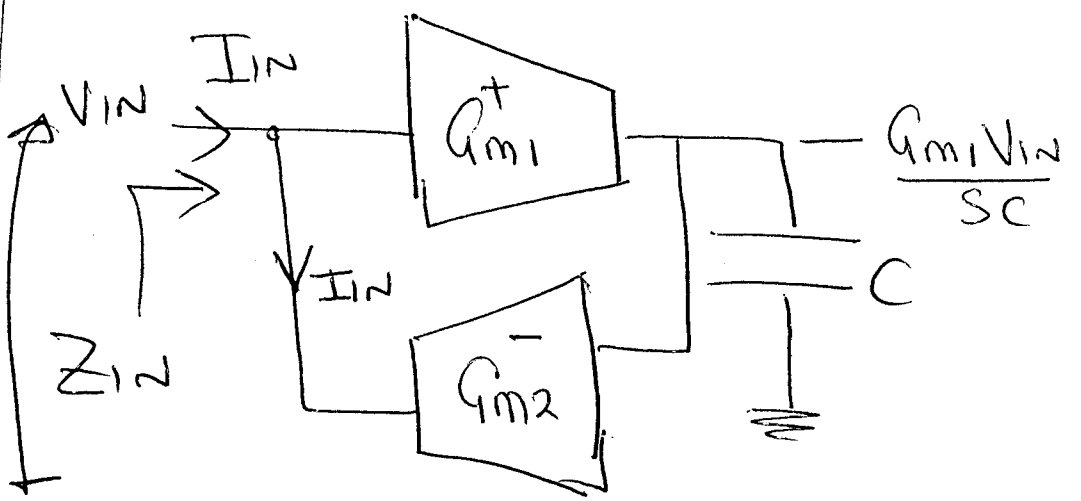
$V_{DS} \geq V_{GS} - V_T$

$V_D = V_S - V_T$

$V_{O(min)} = 2(\Delta V + V_T) - V_T$

$= 2\Delta V + V_T$

Q4



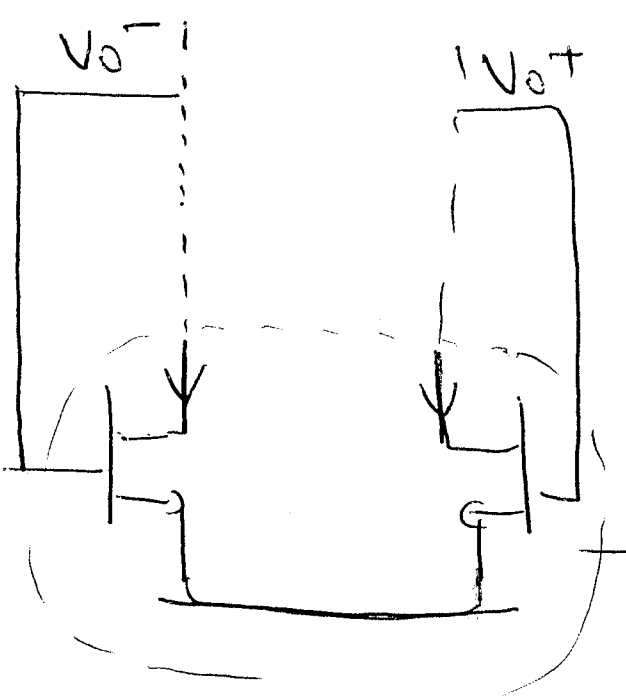
8/8

$$\therefore I_{IN} = \frac{G_{m2}\, G_{m1} V_{IN}}{sC}$$

$$\therefore Z_{IN} = V_{IN}/I_{IN} = s[C/G_{m1}G_{m2}]$$

Hence

$$L = C/(G_{m1}G_{m2})$$



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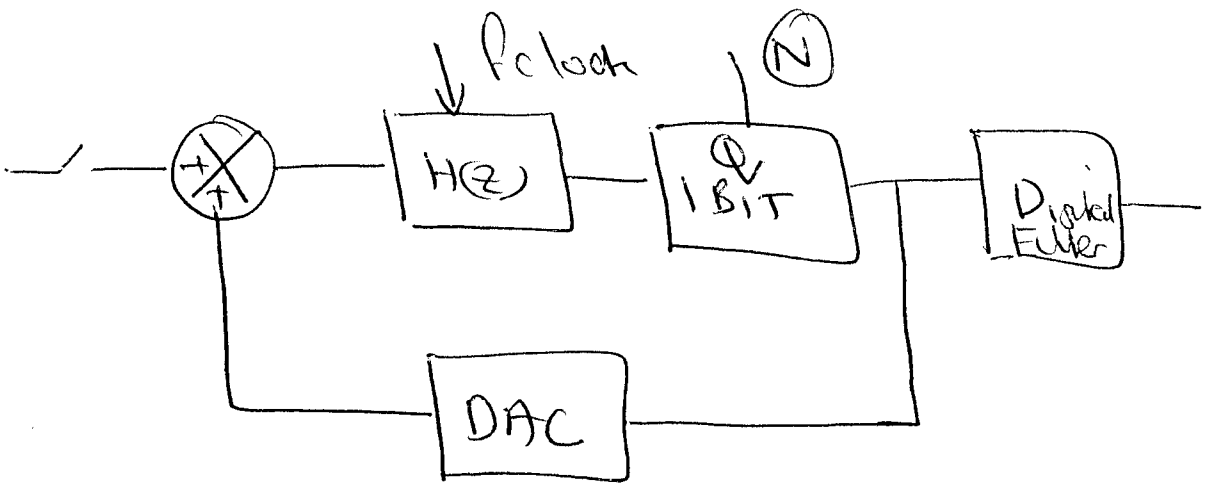
10

Main advantage of folded cascode is low-voltage supply since cascode path is in a vertical and not horizontal plane. Signal swing is reduced but with lower power supply.



Basic idea is that coarse quantisation noise gets shaped by 1/(Hz) via feedback. The feedback DAC and forward integrator force the quantisation error to have a high frequency spectrum. The output of the digital filter is down sampled and given a multibit digital representation. High frequency quantisation noise is reduced. Shaping in noise TF $\simeq \frac{N}{(1+Hz)}$ → Noise shaping.

$$STF = \frac{HN(Hz)}{(1+Hz)} = \text{unity signal gain.}$$

19/10

Q5.

Decoupling Caps

Prevent power supply noise, ripple etc from interfering with output performance Caps act as short-term batteries to wobble on supply. Ceramics quite good. (2/2)

50 ohm

Matches characteristic impedance/resistance of line. Prevents losses in line particularly at high frequency. (2/2)

BNC connector

Provides good coax ground point to input signal source. (2/2)

Ground Plane

Low inductance, low impedance common ground. Prevents ground bounce and high frequency oscillation. Common ground potential throughout board. (2/2)

Algorithmic Converter.

$2I_{IN}$ compares to Iref via input current doubler and reference mirror.

If $2I_{IN} > I_{ref}$ - comparator will go 'high' - digital output 1 and switch Mq will conduct. Analog output will be $2I_{IN} - I_{ref}$ to next bit

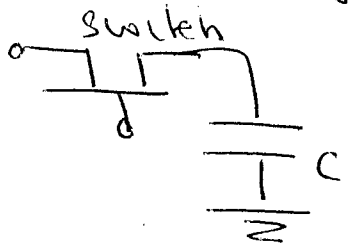
Q5 cont.

If $2I_{IN} < I_{ref}$ → Digital output "0"
Analog output $2I_{IN}$ since MSB is off.
$2I_{IN}$ will then double again to make next synchcat bit. Process continues with n-bits in cascade. The number of cells will determine the resolution of the converter.

Suited to VLSI since can be made with single poly CMOS, no need for linear capacitors.

(9/9)

Dynamic Range DR $\triangleq$ Vref / Noise $= 2^N$



RMS noise of switch driving capacitor $= \sqrt{\frac{kT}{C}}$

$\therefore DR = \frac{V_{ref}}{\sqrt{\frac{kT}{C}}} = 2^N$

Assume $f_c = 1/10R \cdot C$, then solving for C gives

$\therefore DR = 2^N = V_{ref} / \sqrt{kT 10 R f_c}$

(8/8)

Can calculate $R = R_{ON} = \frac{L}{KW[V_{GS} - V_T]}$

from which can calculate DR.

Q6. Advantages of Continuous-time

Speed, simplicity, power consumption

(2/2) Disadvantages

Accuracy, linearity, noise

Figure 6(a)

During ϕ_1 $\quad Q = C_1[V_1 - V_2]$

$I_{av} = f_c C_1 [V_1 - V_2]$

f_c = clock frequency

$\phi_2 \Rightarrow$

$$I_{av} = -f_c C_1 [V_1 - V_2]$$

$$\therefore V_o = \left(\frac{-1}{jwC_2}\right) f_c C_1 [V_1 - V_2]$$

$$\therefore \frac{V_o}{(V_1 - V_2)} = \left[\frac{-f_c C_1}{jw C_2}\right] \Rightarrow \tau = \frac{C_2}{C_1 f_c}$$

(6/6) Accuracy determined by capacitor ratio.

Figure 6(b)

During ϕ_1 $\quad Q = C_1(V_{IN}) \Rightarrow I_{AV} = f_c C_1 V_{IN}$

During ϕ_2

$$I_{av} = -[f_c C_3 V_o + jwC_2 V_o]$$

$$\therefore f_c C_1 V_{IN} = -[f_c C_3 V_o + jwC_2 V_o]$$

$$V_{IN} = -\left[\frac{C_3}{C_1} V_o + \frac{jw C_2}{f_c C_1} V_o\right]$$

(6/6)

Q 6 cont

Recreate

$$\frac{V_o}{V_{IN}} = \left(\frac{C_1}{C_3}\right) \frac{1}{\left(1 + \frac{C_2 j\omega}{C_3 f_c}\right)}$$

$$\Rightarrow \tau = \frac{C_2}{C_3 f_c}$$

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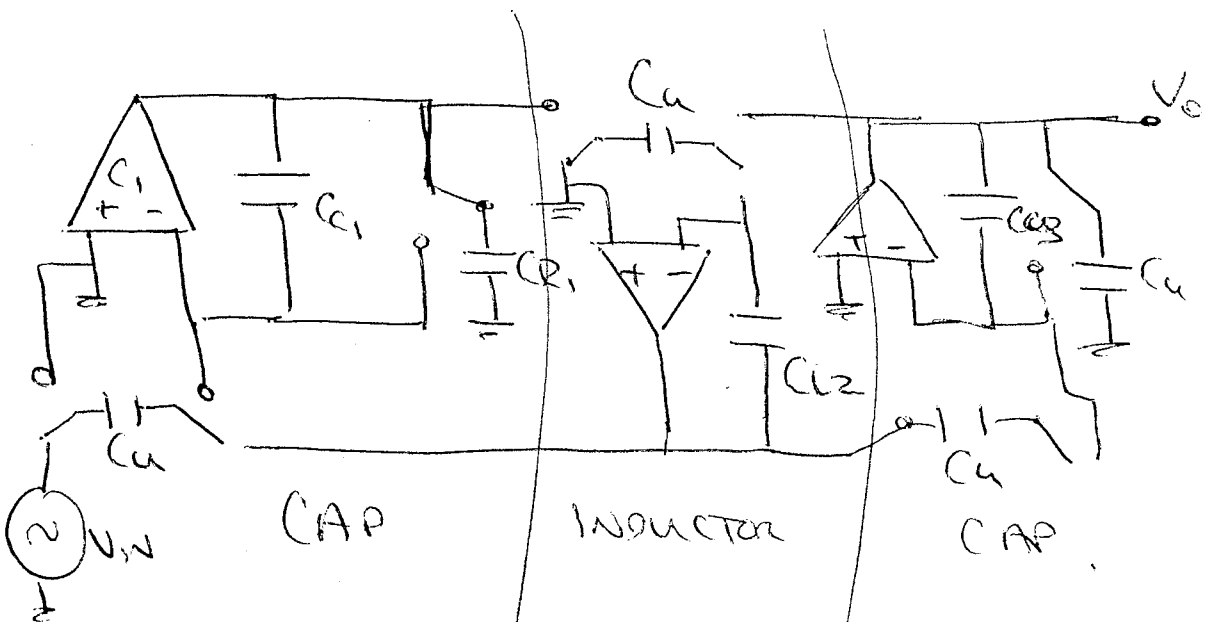
Section of LCR prototype.

General transformation Rules (not really required but the bright students may include)



Conversion into differential integrators.

Inductor transformation

$$(L_2/R_S)f_c = C_{L2}/C_4$$

Capacitor Transformation

$$C_3/C_4 = f_c R_S C_3$$

where R_S is normalizing dummy scaling resistor. Assuming $R_S = 1$

$$\left.\begin{aligned} C_1/C_4 &= f_c C_1 \\ C_{C3}/C_4 &= f_c C_3 \\ C_{L2}/C_4 &= f_c L_2 \end{aligned}\right\} \text{ general transformations.}$$

Table values of C_1, L_2 and C_3 are normalized to 1 rad/s ÷ $2\pi f_p$ (f_p = 5kHz)

$$C_L = C_3 = 2.0236/(2\pi 5\times10^3) = 6.44\times10^{-4}\text{F}$$
$$L_2 = 0.994/(2\pi 5\times10^3) = 3.164\times10^{-4}\text{F}$$

For termination resistors assume $C_{R1} = C_{R2} = 1\text{pF}$

then $\left[\begin{array}{l} C_{L1} = C_{L3} = 6.44\text{pF} \\ C_{L2} = 3.164\text{pF} \end{array}\right]$.

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