IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2007

EEE PART II: MEng, BEng and ACGI

Corrected Copy

ANALOGUE ELECTRONICS 2

Wednesday, 13 June 2:00 pm

Time allowed: 2:00 hours

There are FOUR questions on this paper.

Q1 is compulsory.
Answer Q1 and any two of questions 2-4.
Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible
First Marker(s) : C. Papavassiliou, C. Papavassiliou
Second Marker(s) : E. Rodriguez-Villegas, E. Rodriguez-Villegas

E2.2 ANALOGUE ELECTRONICS

The first question is mandatory.

1. This question consists of 10 brief items. Each item can be answered in a few words or a short paragraph. Please answer all sub-questions, which carry equal marks.

   a) Under what condition is the output impedance of a voltage amplifier independent of the impedance of a signal source connected to its input? [4]

   b) List four of the equivalent ways of describing the small signal behaviour of an amplifier. What is the meaning of gain in each of these descriptions? [4]

   c) Two amplifiers appear in a mail order catalogue. One is listed as a "voltage amplifier" and the other as a "transimpedance amplifier". Which of the two is likely to have a lower input impedance? Justify your answer. [4]

   d) Draw the schematic of a passive second order low pass filter. Write an expression for its transfer function **without** solving the filter circuit. Comment on the magnitude of the quality factor of a passive 2nd order low pass filter. [4]

   e) Describe the common gate amplifier. Draw a schematic for the common gate amplifier and comment on the magnitude of its input and output impedance. Is it better to describe the common gate amplifier as a transimpedance amplifier or as a unity gain current amplifier? Why? [4]

   f) Series-shunt **positive** feedback, with less than unity loop gain, is applied on a voltage amplifier. Will the closed loop amplifier have a higher or lower voltage gain, input impedance and output impedance than the open-loop amplifier? Justify your answer. [4]

   g) Describe the 'Miller Cancellation' technique in high gain and high frequency narrowband applications. In other words, explain how an inductor can used to cancel the effects of the Miller capacitance in a common emitter bipolar transistor amplifier. [4]

   h) A FET transistor has a transit frequency $f_T = 10GHz$. Its threshold voltage is $V_T = 0V$ and its drain current is $I_D = 1mA$ at $V_{GS} = 1V$. Calculate the gate capacitance of this transistor. Calculate the current gain of a common source amplifier built with this transistor at a frequency $f = 1GHz$. You may neglect C_{GD}. [4]

   i) Draw a schematic of a two stage FET amplifier consisting of a common drain stage followed by a common gate stage. What is the common name of this circuit? What are its desirable performance characteristics? [4]

   j) Define the transmission ('ABCD') parameters. Explain how the ABCD parameters are used to simplify multistage amplifier calculations. [4]

[Total: 40]

2. a) Prove that the impedance Z_A between node 'A' and ground in the Generalised Impedance Converter ('GIC'), shown in figure 2.1(a), is given by:

$$Z_A = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \tag{2.1}$$

Assume the op-amps are ideal. [10]

HINT: Apply a test voltage on node 'A' and evaluate the resulting input current.

b) Design a band pass filter with $\omega_0 = 2\pi \times 10kHz$ and $Q = 10$ using only resistors capacitors and operational amplifiers as follows:

i) Calculate the transfer function of the filter in figure 2.1(b). [5]

ii) Calculate L and C to meet the filter specification. $R = 500\Omega$ [5]

iii) Use the generalised impedance converter to emulate the neccessary inductor. Assume the operational amplifiers are ideal. Any capacitors C_G you use must all be equal to the capacitance C you calculated in part (ii) above. All resistors used in the simulated inductor circuit should be of one value R_G (R_G does not need to be equal to R). [5]

iv) Calculate the ratio W_R/W_C. W_R is the energy dissipated on the GIC resistors in one period of the signal at the filter centre frequency. W_C is the peak energy stored on the GIC capacitor(s). [5]

HINT: In 2.b.iii you derived an equation expressing the filter centre frequency in terms of R_G and C_G.

[Total: 30]

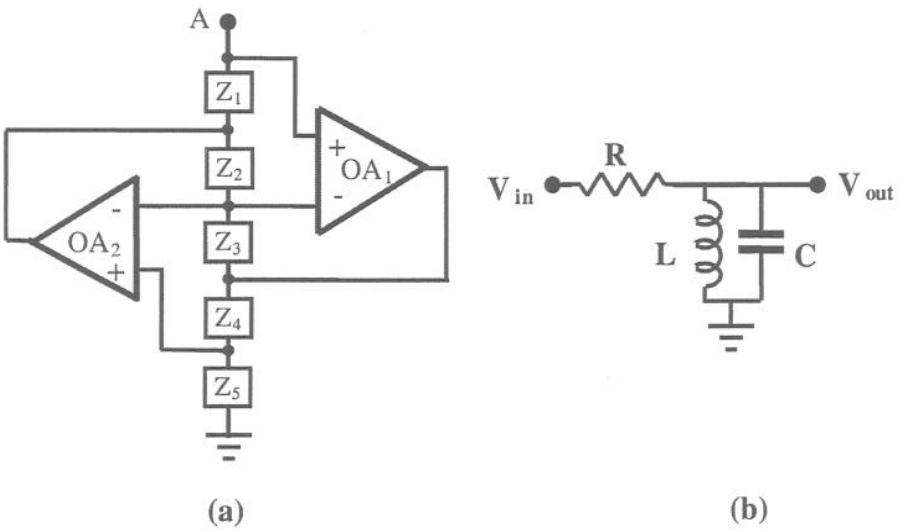


Figure 2.1 (a) Circuit of a Generalised Impedance Converter ('GIC') for question 2.a (b) Band pass filter for 2.b

3. An NPN bipolar transistor has a common emitter current gain $\beta = 100$, a transit frequency $f_T = 1GHz$ and $C_{BE} = 9C_{BC}$ at $I_C = 1mA$. The Early voltage for this transistor is $V_A = 100V$. The thermal voltage at room temperature is approximately $V_{th} = kT/q = 25mV$.

a) Draw the small signal 'Pi' model for the transistor. Identify all elements on this model. [5]

b) Calculate the values of all the small signal model elements appearing in the model of question 3.a. Do your calculation at $I_C = 1mA$. You may ignore C_{CE}. [5]

c) Write by inspection the small signal admittance matrix for the transistor at a DC bias of $I_C = 1mA$ in terms of the transistor 'Pi' model elements. [5]

d) Derive expressions for the entries of the small signal "h" parameter matrix (hybrid, current gain parameters) for this transistor in terms of the admittance parameters you computed in part (c) above. [5]

e) A common emitter voltage amplifier operating at a DC bias of $I_C = 1mA$ and from a supply $V_{CC} = 10V$ has been designed. In this design, shown in figure 3.1, $Z_L = 5k\Omega$ and Z_E as a parallel combination of $R_E = 2k\Omega$ and $C_E = 10nF$.

i) Calculate the transistor common emitter current gain at low frequencies. Use the series form of the Miller theorem to derive an approximate expression for the input impedance of the amplifier of figure 3.1 at low frequencies. [5]

ii) Calculate the voltage gain of this amplifier at high frequencies. Use the parallel form of the Miller theorem to calculate the input impedance of this amplifier at high frequencies. What is the bandwidth of this amplifier if $Z_S = 100\Omega$? [5]

[Total: 30]

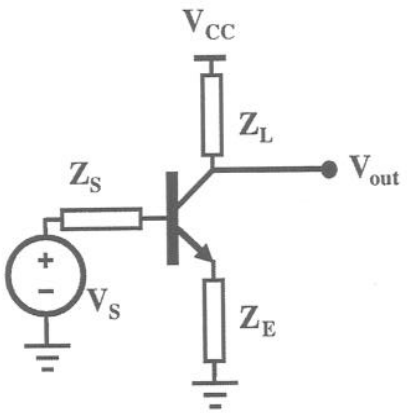


Figure 3.1 The common emitter amplifier for question 3.e

4. The schematic of the Deliyannis-Friend band pass filter is shown in figure 4.1a. For parts (a) and (b) of this question you may assume the op-amp is ideal.

a) Calculate the transfer function of this filter. [5]

b) Express the centre frequency, quality factor and peak gain of this filter in terms of R_1, R_2, C_1 and C_2 . [5]

c) Calculate the transfer function $A = y/x$ of the block diagram in figure 4.1(b). Calculate the sensitivity of this transfer function to the op-amp open loop gain G. [5]

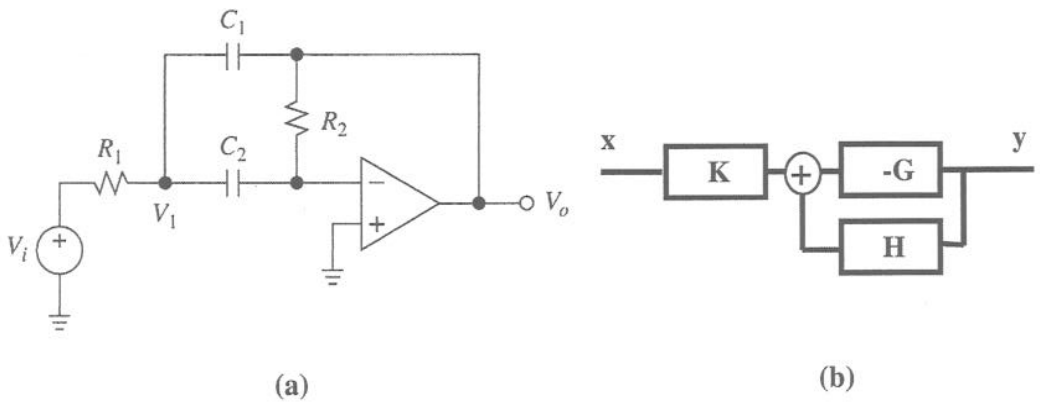
d) Draw a block diagram, similar to that of figure 4.1(b), for a Sallen-Key filter. Derive the transfer function of the Sallen-Key filter. Calculate its sensitivity to the amplifier gain. [5]

e) The finite gain amplifier used in the Sallen-Key filter is implemented using a non-inverting op-amp circuit. Calculate the sensitivity of the amplifier gain on the op-amp gain. Make an approximation to express your answer in terms of the op-amp open loop gain and the amplifier closed loop gain. [5]

f) Compare the sensitivities of the Deliyannis-Friend and Sallen-Key band pass filters to the open loop gain of the op-amp used. Why is the op-amp gain-bandwidth product important in designing active filters? [5]

HINT: The Sallen-Key filter uses positive feedback, and the loop gain is less than unity.

[Total: 30]



(a) (b)

Figure 4.1 (a) The band pass filter for question 4. (b) Model for the filter for question 4.c .

E2.2

2007

SOLUTIONS: -

ANALOGUE ELECTRONICS II

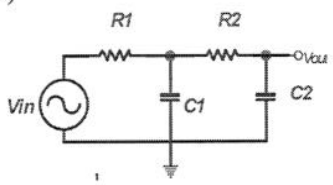
Q1.All taught, except (h) which is computed example]

a) If the amplifier is unilateral. [4]

b) Impedance, Zparameters, gain=transimpedance.
Admittance , Yparameters, Gain is transconductance
Hybrid, Current gain, Hparameters, Gain is Current gain
Reverse hybrid, G parameters, Gain is voltage gain [4]

c) The transimpedance amplifier since is must have a current meter behaviour at the input. [4]

d)



$$H(s)=\frac{1}{s^2+\omega_0 s/Q+1}$$

Q<<1 [4]

e) Common terminal is gate, input at emitter, output at collector. Low input impedance , and hight output impedance. These are the terminal characteristics of a current amplifier. Current gain is unity. [4]

f) Feedback factor F=1-GH< 1. Gain divided by F, increases, input impedance multiplied by F, decreases, output impedance multiplied by F, increases. [4]

g) Connect an inductor between base and collector to resonate C_{BC} at an RF frequency. This makes the amplifier unilateral at that frequency greatly increasing its gain with no bandwidth penalty. [4]

h) $I_D = 1mA = K\left(V_{gs}-V_T\right)^2 \Rightarrow K = 1mA/V^2$

$$g_m = \frac{dI_{DS}}{dV_{gs}} = 2K\left(V_{gs}-V_T\right) = 2\times10^{-3}$$

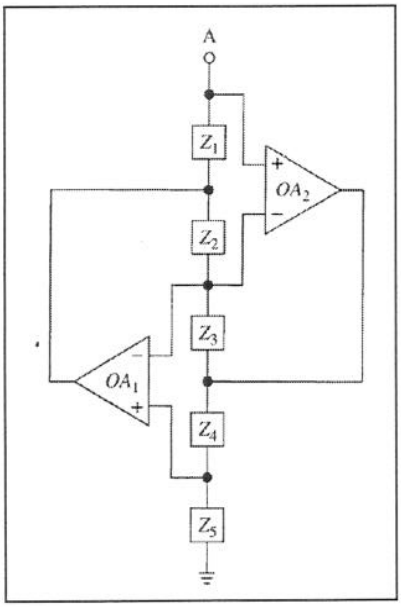
$$f_T = 10^{10} = \frac{g_m}{2\pi C_{gs}} \Rightarrow C_{gs} = \frac{2\times10^{-3}}{2\pi 10^{10}} = 31.9\times10^{-15}\,F$$

At 1GHz the current gain is -10j [4]

i) Differential amplifier. High gain, high bandwidth. [4]

j) $\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}\begin{bmatrix} v_2 \\ -i_2 \end{bmatrix}$. Multiply single stage ABCD matrices to get ABCD of multistage amplifier. [4]

Q2. [new problem, mentioned in notes but not taught]



a) Number the nodes 1,2,3,4,5 from the bottom. Then $V_A = V_5$

$V_5 = V_3 = V_1 \Rightarrow V_1 = V_A \Rightarrow I_1 = V_A / Z_5 \Rightarrow$

$V_2 = V_1 + I_1 Z_4$

$I_2 = (V_2 - V_A)/Z_3$

$V_4 = V_A - I_2 Z_2$

$$I_{in} = (V_A - V_4)/Z_1 = (I_2 Z_2)/Z_1 = (V_2 - V_A)\frac{Z_2}{Z_1 Z_3} = \frac{I_1 Z_4 Z_2}{Z_1 Z_3} = V_A \frac{Z_4 Z_2}{Z_1 Z_3 Z_5} \Rightarrow$$

$$Z_A = \frac{Z_1 Z_3 Z_5}{Z_4 Z_2}$$

[10]

b) [taught procedure]

i)

$$H(s) = \frac{v_{out}}{v_{in}} = \frac{\frac{sL}{1+s^2LC}}{R + \frac{sL}{1+s^2LC}} = \frac{sL}{R}\frac{1}{1+s^2LC+\frac{sL}{R}} \Rightarrow$$

$H_0 = 1$

$\omega_0 = \sqrt{1/LC}$

$Q = R/Z_0$, $Z_0 = \sqrt{L/C}$

[5]

ii)

$$\left.\begin{array}{l}\omega_0 = 1/\sqrt{LC} = 2\pi \times 6 \times 10^4 = 377 \times 10^3 \Rightarrow \sqrt{LC} = 2.65 \times 10^{-6} \\ R/\sqrt{L/C} = 10 \Rightarrow \sqrt{L/C} = 50\end{array}\right\} \Rightarrow$$

$$L = 132\mu H$$

$$C = 53nF$$

[5]

iii) Need to make a L=132nH out of C=53nF. Chose Z2=53nF and resistors elsewhere. Demand

$$\frac{R_1 R_3 R_5 C}{R_4} = L \Rightarrow \frac{R_1 R_3 R_5}{R_4} = \frac{L}{C} = 2500$$

Any way to achieve this is acceptable. If we require all resistors equal, then R=50 Ohm.

[5]

iv) [first year material!]

$$i_{Z1} = i_A = V_A / \omega L = V_A / 50$$

$$P_{total} = P_{Z1} + P_{Z2} + P_{Z3} + P_{Z4} + P_{Z5}$$

all currents are equal in magnitude, and there is no dissipation on Z2. Therefore:

$$P_{total} = 4I^2 R = 4V_A^2 / R$$

In one period, $W_R = / \frac{4\pi V_A^2}{\omega_0 R}$ where V_A is the signal amplitude, while the peak energy stored on the capacitor is $W_C = \frac{1}{2} C V_A^2$

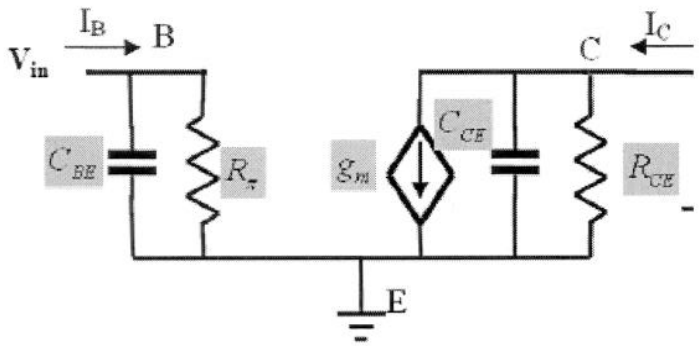
The ratio of the two energies is:

$\frac{W_C}{W_R} = \frac{\omega_0 RC}{8\pi}$. since $\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{RC}$ it follows that $\frac{W_C}{W_R} = \frac{1}{8\pi}$.

[5]

Q3.

a) [bookwork]



[5]

b) [taught procedure]

$$\left.\begin{aligned} f_T &= \frac{g_m}{2\pi\left(C_{BE}+C_{BC}\right)} = \frac{g_m}{20\pi C_{BC}} \\ g_m &= \frac{i_c}{V_{th}} = \frac{1mA}{25mV} = 40mS \end{aligned}\right\} \Rightarrow C_{BC} = \frac{40mS}{20\pi\times 10^9} 636.6\,fF \Rightarrow$$

$$C_{BE} = 9C_{BC} = 5.73\,pF$$

$$R_\pi = \beta / g_m = \frac{100}{0.04} = 2500$$

$$R_{CE} = \frac{V_A}{1mA} = 100k\Omega$$

[5]

c) [taught procedure]

i) $\mathbf{Y} = \begin{bmatrix} s\left(C_{BE}+C_{BC}\right)+1/R_\pi & -sC_{BC} \\ g_m - sC_{BC} & 1/R_A + sC_{BC} \end{bmatrix}$

[5]

ii) [similar to coursework example]
from Y calculate H:

$$\begin{bmatrix} v_1 \\ i_2 \end{bmatrix} = h\begin{bmatrix} i_1 \\ v_2 \end{bmatrix} \Rightarrow \begin{bmatrix} 1 & 0 \\ y_{21} & y_{22} \end{bmatrix} = h\begin{bmatrix} y_{11} & y_{12} \\ 0 & 1 \end{bmatrix} \Rightarrow$$

$$h = \begin{bmatrix} 1 & 0 \\ y_{21} & y_{22} \end{bmatrix}\begin{bmatrix} y_{11} & y_{12} \\ 0 & 1 \end{bmatrix}^{-1} = \frac{1}{y_{11}}\begin{bmatrix} 1 & 0 \\ y_{21} & y_{22} \end{bmatrix}\begin{bmatrix} 1 & -y_{12} \\ 0 & y_{11} \end{bmatrix} = \frac{1}{y_{11}}\begin{bmatrix} 1 & -y_{12} \\ y_{21} & \Delta y \end{bmatrix}$$

[5]

iii) [application of taught theory]

$h_{21} \simeq \beta$

The series form of the Miller theorem suggests that

$$Z_{in}' = Z_{in} + \left(h_{21}+1\right)Z_E = R_\pi // C_{BE} + \left(1+\beta\right)\left(R_E // C_E\right)$$

[5]

iv) [application of taught theory]
The parallel form of the Miller theorem suggests that

$$\left.\begin{aligned} Y_{in} &= Y_0 + (G+1)C_{BC} \\ G &= g_m R_c = 5k\Omega \times 40mS = 200 \end{aligned}\right\} \Rightarrow Y_{in} \simeq C_{BE} + 201C_{BC} \simeq 134pF$$

The dominant pole will then be at

$$f_o = \frac{1}{2\pi R_S \left(C_{BE} + (G+1)C_{BC}\right)} = 11MHz$$

[5]

Q4) [computed example, known circuit, not taught]

a)

$$\left.\begin{array}{l}(V_o-V_1)sC_1+(V_i-V_1)G_1-V_1sC_2=0\Rightarrow V_o s\tau_1+V_i-V_1(s\tau_1+1+s\tau_{12})=0\\ V_oG_2+V_1sC_2=0\Rightarrow V_1=-V_oG_2/sC_2=-V_o/s\tau_2\end{array}\right\}\Rightarrow$$

$$V_o s\tau_1+V_i+V_o(s\tau_1+1+s\tau_{12})/s\tau_2=0\Rightarrow$$

$$\frac{V_o}{V_i}=\frac{-1}{s\tau_1+(s\tau_1+1+s\tau_{12})/s\tau_2}=\frac{-s\tau_2}{s^2\tau_1\tau_2+s(\tau_1+\tau_{12})+1}=\frac{-\tau_2}{\tau_1+\tau_{12}}\frac{s(\tau_1+\tau_{12})}{s^2\tau_1\tau_2+s(\tau_1+\tau_{12})+1}$$

[5]

b) [taught and practiced procedure]

$$H_0=\frac{-\tau_2}{\tau_1+\tau_{12}}$$

$$\omega_0=\frac{1}{\sqrt{\tau_1\tau_2}}$$

$$\zeta=\frac{1}{2}\frac{\tau_1+\tau_{12}}{\sqrt{\tau_1\tau_2}}=\frac{1}{Q}$$

Note that

$$|Q|=2H_0\sqrt{\frac{\tau_1}{\tau_2}}$$

[5]

c) [application of theory]

i)

$$A_v=\frac{y}{x}=\frac{-KG}{1+GH}$$

$$\lim_{G\to\infty}\frac{y}{x}=\frac{-K}{H}$$

$$S_{Av,G}=\frac{G}{A_v}\frac{\partial}{\partial G}\left(\frac{-KG}{1+GH}\right)=\frac{G}{A_v}\frac{-K(1+GH)+KGH}{(1+GH)^2}=\frac{1}{1+GH}<<1$$

[5]

d) [diagram taught]

Same diagram, except G is positive and finite!

Therefore same sensitivity function, accounting for positive feedback,

$$S_{Av,G}=\frac{G}{A_v}\frac{\partial}{\partial G}\left(\frac{-KG}{1-GH}\right)=\frac{G}{A_v}\frac{-K(1+GH)+KGH}{(1-GH)^2}=\frac{1}{1-GH}>1$$

[5]

e) [taught]
The non-inverting amplifier is again a feedback circuit, so

$$G_0 = \frac{G}{1+GH} \Rightarrow S_{Go,G} = \frac{G}{G_0}\frac{\partial G_0}{\partial G} = \frac{G}{G_0}\frac{1+GH-GH}{(1+GH)^2} = \frac{1}{1+GH}$$

$$H = \frac{1}{G_0} \Rightarrow S = \frac{G_0}{G_0+G} \simeq \frac{G_0}{G}$$

[5]

f) [interpretation]
The overall sensitivity of the SK filter is:

$$S_{F,G} = S_{F,G_0} S_{G_0,G} = \frac{1}{1-GH}\frac{G_0}{G} > \frac{G_0}{G}$$

While the sensitivity of the DF filter is

$$S = \frac{1}{1+GH} \approx \frac{1}{GH} \simeq \frac{1}{G}$$

So the DF filter is less sensitive to the op-amp gain.
The gain bandwidth product determines the open op-amp loop gain at the signal frequency.
[5]