Master

E2.2

IMPERIAL COLLEGE LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2006

EEE PART II: MEng, BEng and ACGI

Corrected Copy

ANALOGUE ELECTRONICS 2

Monday, 5 June 2:00 pm

Time allowed: 2:00 hours

There are FOUR questions in this paper.

Q1 is compulsory
Answer Q1 and any two of questions 2-4.
Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Any special instructions for invigilators and information for candidates are on page 1.

Examiners responsible	First Marker(s):	C. Papavassiliou
	Second Marker(s):	E. Rodriguez-Villegas

1. **(compulsory)**

a) An amplifier is given with a voltage gain of $A_v = 10$. An engineer manages, with a suitable feedback connection, to raise the voltage gain to $A_v = 100$. Is the connection used a positive or a negative feedback connection? How much is the loop gain of this connection? Explain your answer. [5]

b) A transconductance amplifier is given with an input impedance of 1 kΩ and an output impedance of 100 Ω. An input impedance of 1 MΩ is required, and negative feedback implemented with resistors is used to do this. What is the loop gain required, and consequently what is the minimum gain the amplifier can have for this to be possible using only passive elements in the feedback connection? [5]

c) Explain why the input impedance of a loaded amplifier changes as we change the load impedance connected to its output. [5]

d) Which type of two stage transistor amplifier would you prefer to use in an application requiring a large voltage gain and a large bandwidth at the same time? Show your reasoning. [5]

e) Considering that all MOSFET transistors have a finite transit frequency, what is the current gain of a MOSFET with $f_T = 1$ GHz if this MOSFET is used as a common source, small signal current amplifier at $f = 100$ MHz? What is the phase of the current gain? Show your calculations. [5]

f) A second year student designed an operational amplifier which has a dominant pole at $f = 10$Hz and a DC open loop voltage gain of $A_V = 10^3$. Calculate the maximum voltage gain an audio preamplifier built with this op-amp using resistive feedback can have at a frequency of $f = 10$ kHz. Show your calculations. [5]

g) An audio application requires a high order low pass filter at 24 kHz to exhibit a 96dB attenuation relative to the passband gain at 48kHz. Using a Bode plot, or otherwise, calculate the minimum order of the filter required to meet this specification. [5]

h) An audio power amplifier delivers 75W RMS to an 8 ohm load when driven by a 10 V peak-to-peak sinusoid. Upon inspection you find that the DC power supply inside the amplifier delivers a maximum of 1 A at 48 V. Calculate power gain, voltage gain and input impedance of this amplifier. (The RMS amplitude of a sinusoid of amplitude V_0 is $V_0/\sqrt{2}$). HINT: apply conservation of power. [5]

2. A student proposed to use the circuit in Figure 2.1 as a high pass filter. The student argued that the capacitor in the feedback path will supply an increasing with frequency current to R_3. As a result, the overall gain will increase with frequency. In this problem you will check the student's claims by analysing the circuit. As this circuit is rather complicated, we take a step-by-step approach.

a) Calculate the ideal frequency response of this filter assuming the op-amp is ideal.

[10]

b) Model the circuit of Figure 2.1 as a block diagram similar to that of Figure 2.2. Calculate the gains of the blocks B and H.

[10]

c) Use the block diagram of part b) to calculate the frequency response of this filter with a realistic op-amp of finite gain-bandwidth product. Assume the DC gain and dominant pole location of the op-amp have been provided. The op-amp is otherwise ideal. What type of filter is this? Calculate its centre frequency, quality factor and maximum gain. [10]

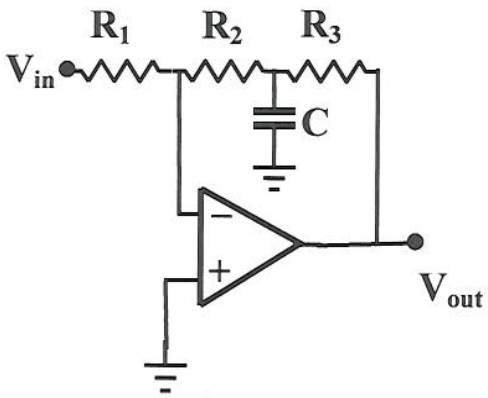

Figure 2.1

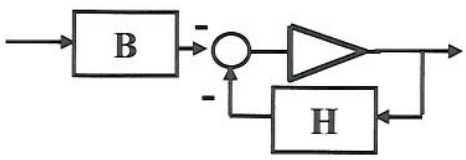

Figure 2.2

3. In this problem you will complete the design of the 100 MHz bandpass radio frequency amplifier shown in Figure 3.1. The following data are given for the transistor:

Symbol	Condition	Value	Units
β	$10mA > I_C > 0.1mA$	50	---
C_{BE0}	$V_{BE} = 0$	1	pF
f_T	$I_C = 1mA$	5	GHz
C_{BC}	$V_{BC} = 0V$	0.1	pF
V_A	$V_{CE} > 0.2V$	40	V
C_{CE}	$V_{CE} > 0$	0	pF

a) Choose a suitable value for R_E so that you have sufficient information to construct a small signal model of the transistor. [2]

b) Draw the small signal equivalent circuit of the amplifier, clearly identifying all elements of the transistor equivalent circuit and all circuit components. Calculate the values of all equivalent circuit elements. You may assume the depletion capacitances have no bias dependence. [8]

c) Choose values for C_E and C_B so these two capacitors are effectively shorted at the amplifier design frequency. You may interpret the term "effectively shorted" to mean that the capacitor admittance must be at least 100 times higher than the total of any admittances connected to it. [5]

d) Choose a value for L_F so that it completely neutralizes the Miller capacitance C_{BC} at the design frequency. Why is this important? [5]

e) Calculate the maximum possible voltage gain of this amplifier when driven by a 50 Ω source at the 100 MHz design frequency, by letting $L_C \to \infty$. [5]

f) Calculate a value for L_C so the voltage gain of this amplifier at 100 MHz is $A_v = 20$ when driven by a 50 Ω FM antenna. What is the phase of the gain? [5]

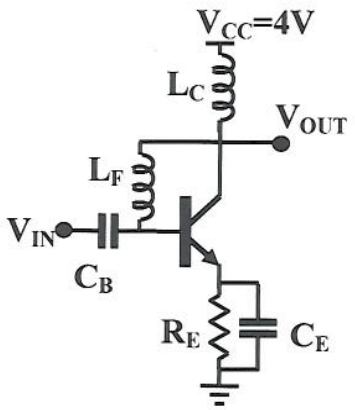

Figure 3.1

4. Two small signal amplifiers are available, with the following parameter matrices:

a transconductor with

$$Y_1 = \begin{bmatrix} A(1+s\tau_A) & C \\ B & D \end{bmatrix}$$

and a voltage amplifier with

$$G_2 = \begin{bmatrix} E(1+s\tau_E) & G \\ \dfrac{F}{1+s\tau_E} & H \end{bmatrix}$$

The constants appearing in these matrices have the values in Table 4.1:

Symbol	A	τ_A	B	C	D	E	τ_E	F	G	H
Value	2×10^{-4}	10^{-7}	2×10^{-3}	10^{-3}	10^{-4}	10^{-3}	10^{-6}	50	0	50
Units	?	?	?	?	?	?	?	?	?	?

Table 4.1

a) Write down the units for all the entries of table 4.1

[5]

b) Draw equivalent circuits for each of the two amplifiers described by Y_1 and G_2. Only resistors, capacitors, inductors and controlled sources can appear in your equivalent circuits.

[6]

c) Is any of the two amplifiers unilateral? Explain your answer.

[4]

d) What is the total voltage gain of a system in which a 500 Ω Thevenin source drives amplifier Y_1, which in turn drives amplifier G_2 and which finally drives a 100 Ω load?

HINT: You must account for the effect a load can have on an amplifier's input impedance.

[15]

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ANSWER Q1:

a) The closed loop gain of a feedback connected amplifier is $G_{CL} = \frac{G}{1-GH}$. Since the feedback connection increases the gain the denominator must be less than 1, i.e. the feedback connection is positive. The loop gain is $GH = 0.9$

b) The input impedance of the amplifier is required to increase by a factor of 1000. A series input negative feedback connection increases the input impedance to $Z_{in}^{'} = Z_{in0}(1+GH)$. Then $GH = 999$. Since $H < 1$ for a resistive network it follows $G > 999$

c) A realistic amplifier has reverse gain. The reverse gain, together with the load and the output impedance can be modelled as a feedback network. Since the input impedance depends on the loop gain and the loop gain depends on the load, it follows that the input impedance depends on the load.

d) The cascode, because it exhibits the large voltage gain of the CE first stage, while the CB second stage almost eliminates the bandwidth limiting Miller feedback.

e) The small signal current gain of a MOSFET at any frequency is $h = \frac{g_m}{2\pi(C_{gs}+C_{be})j\omega} \Rightarrow |h| = \frac{f_T}{f}$. For the numbers given, $|h| = 10$.

The phase is -90 degrees.

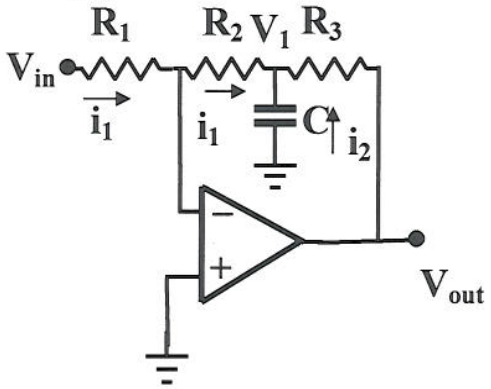
f) This is a dominant pole amplifier with $GBP = 10^4$. The maximum gain a resistive negative feedback circuit built around it can have at 10kHz is 1.

g) 96dB attenuation at double the pole frequency means $10^{4.6} = 2^N \Rightarrow N > 15.95$. The minimum filter order required is 16.

h) The power supply can deliver a maximum of 48W. Then, a minimum 27 W must come from the signal input. The power gain is therefore less than $G_{P\max} < \frac{48}{27} = 1.78$. The output voltage, in order to deliver 75 W must have an amplitude: $\frac{1}{2R_L}V_{out}^2 = 75 \Rightarrow V_{out} = \sqrt{1200} = 34.6$, and twice this value peak-to-peak. So the voltage gain must be 6.92. The input impedance must be: $\frac{1}{2R_{in}}(5)^2 > 27 \Rightarrow R_{in} < \frac{25}{54} = 0.45\ \Omega$. This looks like a transimpedance amplifier.

[40]

ANSWER Q2 [Computed example]:



a)
In the following $G_i = 1/R_i$.

let $V_{out} = FV_{in}$

$V_- = 0$

$i_1 = V_{in}G_1$

$V_1 = -i_1R_2 = -V_{in}G_1R_2$

$i_2 = -V_1sC = V_{in}G_1R_2sC$

$V_{out} = V_1 - (i_1 + i_2)R_3 = -V_{in}G_1R_2 - (V_{in}G_1 + V_{in}G_1R_2sC)R_3 =$

$= -V_{in}(G_1R_2 + G_1R_3 + G_1R_2sCR_3) \Rightarrow F = -(G_1R_2 + G_1R_3 + G_1R_2sCR_3) \Rightarrow$

$F = -F_0(1 + s\tau)$

with

$$F_0 = G_1(R_2 + R_3)\ ,\ \tau = \frac{R_2R_3C}{R_2 + R_3}$$

This is a lossy differentiator. [10]

b) The closed loop gain we just calculated is equal to:

$$F = \lim_{A\to\infty} \frac{-AB}{1 + AH} \Rightarrow F = \frac{-B}{H} = -F_0(1 + s\tau)$$

B is the input voltage divider:

$$B=\frac{R_2+R_3\,//\,C}{R_1+R_2+R_3\,//\,C}=\frac{R_2+\dfrac{R_3}{1+R_3sC}}{R_1+R_2+\dfrac{R_3}{1+R_3sC}}=$$

$$=\frac{R_2\left(1+R_3sC\right)+R_3}{\left(R_1+R_2\right)\left(1+R_3sC\right)+R_3}=\frac{R_2+R_3+R_2R_3sC}{R_1+R_2+R_3+\left(R_1+R_2\right)R_3sC}=B_0\frac{1+s\tau_{BZ}}{1+s\tau_{Bp}}\text{ with}$$

$$B_0=\frac{R_2+R_3}{R_1+R_2+R_3}<1\ ,\ \tau_{BZ}=\frac{R_2R_3c}{R_2+R_3}=\tau\ ,\ \tau_{Bp}=\frac{\left(R_1+R_2\right)R_3C}{R_1+R_2+R_3}$$

we can now get H,

$$H=\frac{B}{F_0\left(1+s\tau\right)}=\frac{B_0}{F_0\left(1+s\tau_{Bp}\right)}$$ [10]

c)

$$F=\frac{-A(s)B(s)}{1+A(s)H(s)}\text{ with}$$

$$\mathrm{A(s)}=\frac{A_0}{1+s\tau_0},\ \mathrm{B}=B_0\frac{1+s\tau}{1+s\tau_{Bp}}\text{ and }\mathrm{H(s)}=\frac{B_0}{A_0\left(1+s\tau_{Bp}\right)}$$

$$\Rightarrow F=-\frac{\dfrac{A_0}{1+s\tau_0}B_0\dfrac{1+s\tau}{1+s\tau_{Bp}}}{1+\dfrac{A_0}{1+s\tau_0}\dfrac{B_0}{F_0\left(1+s\tau_{Bp}\right)}}=-\frac{F_0A_0B_0\left(1+s\tau\right)}{F_0\left(1+s\tau_{Bp}\right)\left(1+s\tau_0\right)+A_0B_0}=$$

$$=\frac{-F_0A_0B_0}{F_0+A_0B_0}\frac{1+s\tau}{\left(s^2\tau_0\tau_{Bp}F_0/\left(F_0+A_0B_0\right)+\left(\tau_{Bp}+\tau_0\right)F_0/\left(F_0+A_0B_0\right)+1\right)}$$

This is the sum of a second order LPF and a BPF.

$$\omega_0=\sqrt{\frac{F_0+A_0B_0}{F_0\tau_{Bp}\tau_0}}$$

$$2\zeta/\omega_0=\frac{F_0\left(\tau_{Bp}+\tau_0\right)}{F_0+A_0B_0}\Rightarrow\zeta=\frac{1}{2}\frac{F_0\left(\tau_{Bp}+\tau_0\right)}{F_0+A_0B_0}\sqrt{\frac{F_0+A_0B_0}{F_0\tau_{Bp}\tau_0}}\Rightarrow$$

$$\Rightarrow\zeta=\frac{1}{2}\sqrt{\frac{F_0}{F_0+A_0B_0}}\left(\sqrt{\frac{\tau_{Bp}}{\tau_0}}+\sqrt{\frac{\tau_0}{\tau_{Bp}}}\right)\square\ 1$$

The maximum gain is $H_0=\sqrt{2}\dfrac{F_0A_0B_0}{F_0+A_0B_0}\rightarrow\sqrt{2}F_0$ [10]

ANSWER Q3 [design problem]

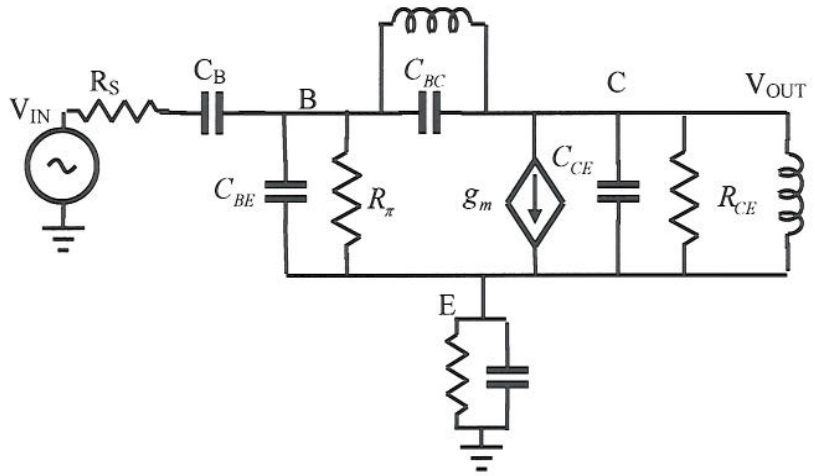
a) Operating point: we want $I_C = 1mA$.

$I_E = 1.02mA$

Then, $V_E = I_E R_E$ Then R_E=3.3k [2]

$V_C = 0.7 + I_E R_E$

b)



$$R_\pi = \beta \frac{V_{th}}{I_C} = 1.3k\Omega$$

$$g_m = \frac{I_C}{V_{th}} = 38.4mS$$

$$C_{BC} = C_{BC0} = 0.1pF$$

$$C_{BE} + C_{CE0} = \frac{g_m}{2\pi f_T} = \frac{38.4mS}{2\pi \times 5GHz} = 1.22pF \Rightarrow C_{BE} = 1.12pF$$

$$R_{CE} = \frac{V_A}{I_C} = 40k\Omega$$ [8]

c) We can chose C_E to be negligible compared to 1/gm at the peak frequency. Negligible means that

$$\omega C_E > 100 g_m \Rightarrow C_E > 100\omega_T / \omega \left(C_{BE} + C_{BC0}\right) \Rightarrow$$
$$C_E > 50 = 100 * 1.22pF = 6.10nF$$ [3]

The input DC blocking capacitance to be negligible compared to the source impedance, so that:

$$\omega C_B > 100/50 \Rightarrow \cdots \Rightarrow C_B > 12nF$$ [2]

d) The Miller neutralisation at 100 MHz requires that we choose:

$100MHz = \frac{1}{2\pi\sqrt{L_F C_{BC}}} \Rightarrow L_F = 25.3\mu H$ At the centre frequency the amplifier is unilateral.

[5]

e) The maximum possible amplifier gain from an ideal voltage source at 100MHz is just:

$$A_V = -\frac{g_m\left(R_{CE} // j\omega L_C\right)}{1 + jR_S\omega C_{BE}} \Rightarrow$$

$$\max\left|A_V\right| = \frac{g_m R_{CE}}{R_S\omega C_{BE}} = \frac{0.039\times 40k}{50\times 159M\text{rad/s}\times 1.2pF} = 163.5$$

[5]

f)

If a gain of 20 is required then

$$\frac{g_m\omega L_C}{R_S\omega C_{BE}} = 20 \Rightarrow L_C = 5000/159Mrad/ = 31.4\mu H$$

[5]

ANSWER, Q4

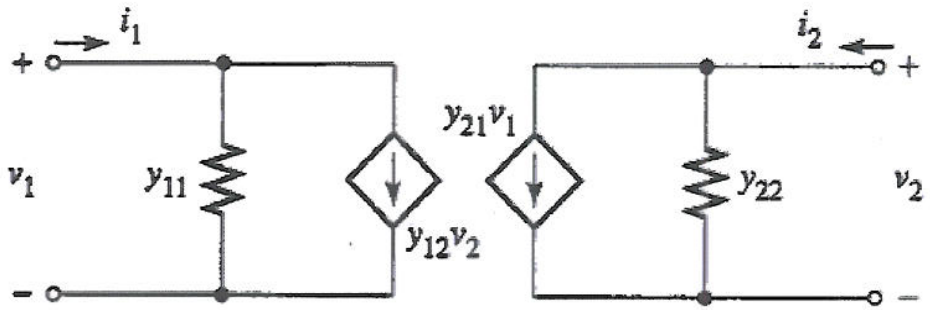
a) [bookwork]

Symbol	A	τ_A	B	C	D	E	τ_E	F	G	H
Value	2×10^{-4}	10^{-7}	2×10^{-3}	10^{-3}	10^{-4}	10^{-3}	10^{-6}	50	0	50
Units	S	sec	S	S	S	S	sec	--	--	Ω

[5]

b) [bookwork]

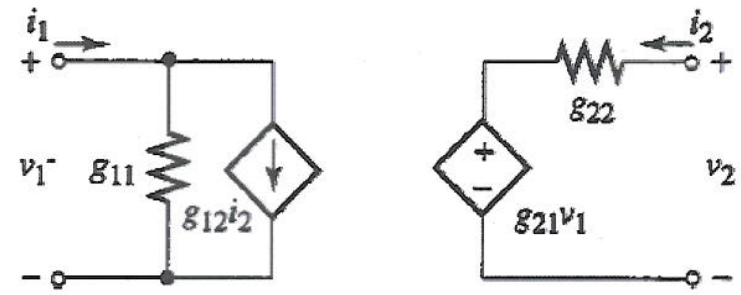
the first is a Norton-Norton:



the matrix entries corresponding to $Y_1 = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$

Y_{11} is a parallel RC network with $R = 1/A = 5k\Omega$, $C = A\tau_A = 20pF$ [3]

The second amplifier is a Norton – Thevenin:



The matrix entries corresponding to: $G_2 = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix}$

G_{11} is a parallel RC network with $R = 1/E = 1k\Omega$, $C = E\tau_E = 1nF$ [3]

c) [bookwork] The Y amplifier is unilateral since $y_{12} = 0$. The G amplifier is not since $g_{12} \neq 0$. [4]

d) [computed example]

The following must be taken into account:

i) Convert the transconductor into a voltage amplifier of gain $G_1 = -g_m / g_{out} = -B/D$.

ii) calculate the voltage divider $D_1 = \dfrac{1}{1 + R_s A\left(1 + s\tau_A\right)}$ from the source to the transconductor input.

iii) calculate the loaded input admittance Yin' of the second stage voltage amplifier:

$$\left.\begin{aligned} i_1 &= g_{11}v_1 + g_{12}i_2 = g_{11}v_1 - g_{12}g_L v_2 \\ v_2 &= g_{21}v_1 + g_{22}i_2 = g_{21}v_1 - g_{22}g_L v_2 \Rightarrow \\ v_2\left(1 + g_{22}g_L\right) &= g_{21}v_1 \Rightarrow v_2 = \frac{g_{21}}{1 + g_{22}g_L}v_1 \end{aligned}\right\} \Rightarrow$$

$$i_1 = v_1\left(g_{11} - \frac{g_{12}g_{21}}{1 + g_{22}g_L}\right) \Rightarrow Y_{in}^{'} = g_{11} + \frac{g_{11}g_{22} - g_{12}g_{21}}{1 + g_{22}g_L}$$

iv) calculate the voltage divider $D_2 = \dfrac{1}{1 + Y_{in}^{'}/D}$ from the transconductor output to the modified voltage amplifier input admittance

v) Calculate the voltage divider $D_3 = \dfrac{1}{1 + HR_L}$ from the output of the second stage to the load.

The overall gain required is clearly:

$A_V = G_1 G_{21} D_1 D_2 D_3$

[15]