Paper Number(s): **E2.2**

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2001

EEE PART II: M.Eng., B.Eng. and ACGI

ANALOGUE ELECTRONICS II

Monday, 4 June 2:00 pm

There are FIVE questions on this paper.

Answer THREE questions.

Time allowed: 2:00 hours

Corrected Copy

NONE

Examiners: Toumazou,C. and Papavassiliou,C.

1. Use the circuit of *Figure 1a* to confirm Miller's theorem by deriving expressions for the input and output admittance of the network. [6]

For the circuit of *Figure 1b* apply Miller's theorem to estimate the high frequency, small signal – 3dB bandwidth of the amplifier, given the following transistor data for a collector current of 1mA:

$V_{BE(on)} = 660$ mV $kT/q = 26$ m V at room temperature,
$\beta = 100$ $E_a = 100$ $r_{b'b} = 50\ \Omega$ $C_{b'c} = 2$pF
$I_S = 9.45 \times 10^{-15}$ A $f_T = 430$ MHz

Assume the input side of the amplifier dominates the bandwidth.

[14]

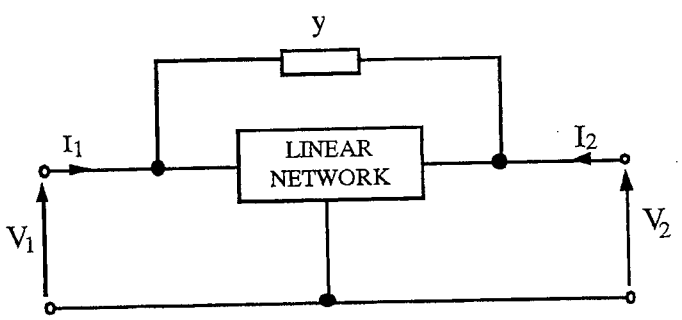


Figure 1a

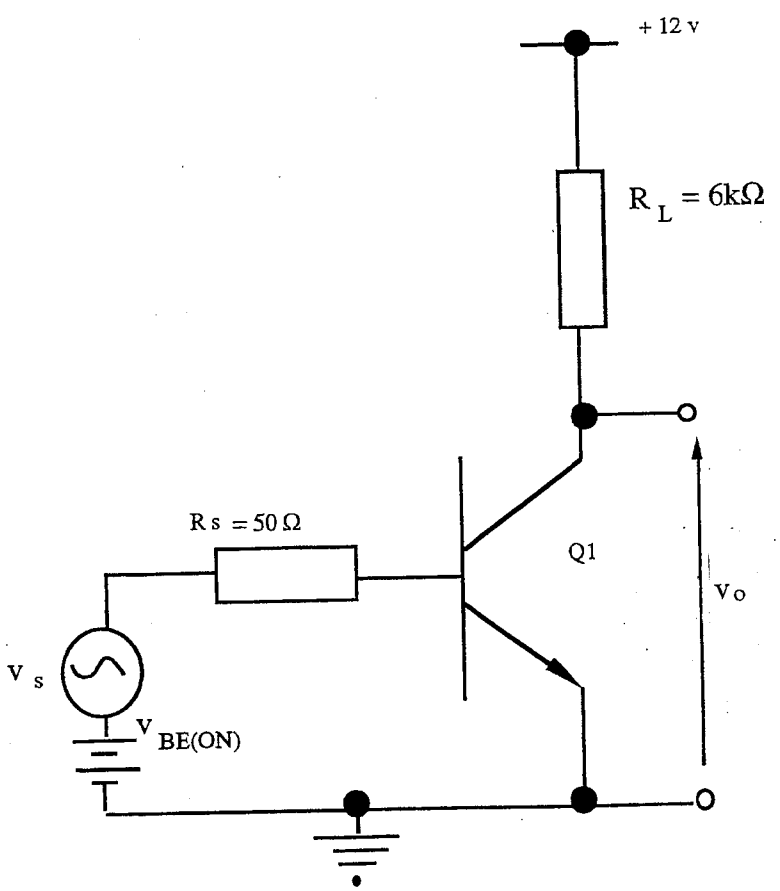


Figure 1b

2. *Figure 2* shows a single-stage inverting CMOS voltage amplifier.

The CMOS process has the following parameters:

NMOS	PMOS
$K_N = 20\mu A/V^2$	$Kp = 10\mu A/V^2$
$\lambda_N = 0.01$	$\lambda p = 0.02$
$VT_N = +2V$	$VTp = -2V$

Given that the process has a fixed transistor gate length, show that the small signal voltage gain of the amplifier is given by

$$Av = -94.3\ (W1/W2)^{1/2}$$

Where W1 and W2 are the channel widths of NMOS transistor Q1 and PMOS transistor Q2 respectively. You may assume a value of $V_{bias} = 2V$ and you may further assume that the d.c. value of V_{in} is appropriate for correctly biasing the amplifier. [15]

Finally, what is meant by the BODY EFFECT of the transistor and what precautions are taken to reduce the effect in a practical circuit such as that of *Figure 2* ? [5]

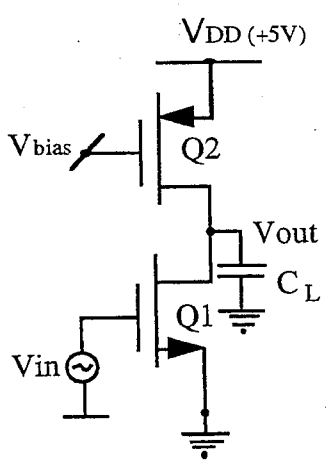


Figure 2

3. Briefly explain what is meant by the terms 'cascoding' and 'bootstrapping' when applied to CMOS amplifiers. [6]

Figure 3 shows a single-cascode, inverting CMOS amplifier. Using simplified small-signal models for each FET prove that the output conductance of the amplifier is given by:

$$g_{out} \approx [(g_{o1} g_{o2})]/g_{m2}] + [(g_{o4} g_{o3})/g_{m3})]$$

where g_o is the output conductance and g_m the transconductance of the FET. State any assumptions you make. [10]

Given that the threshold voltage of the PMOS device is –2 V, estimate the maximum positive output swing of the amplifier of *Figure 3.* [4]

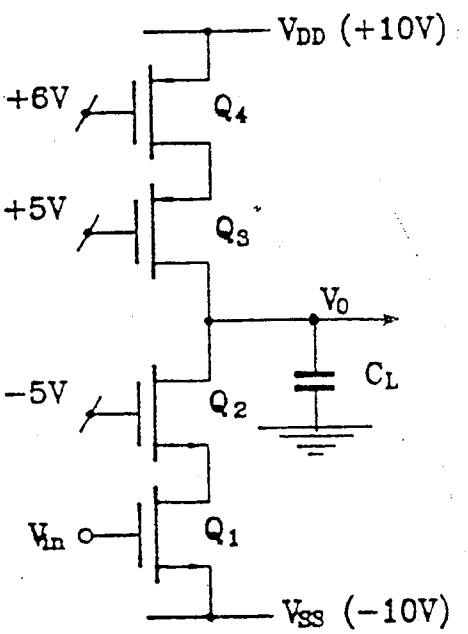


Figure 3

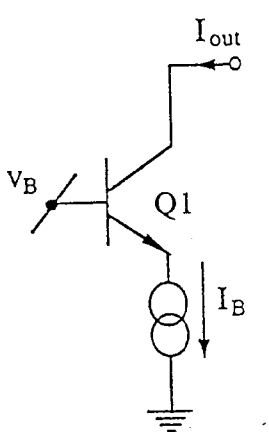
4. Give two reasons why is it necessary in analogue electronics to create current –sources and current-sinks with high output resistance. [2]

Figure 4 shows the circuits of two current sources each biased appropriately with a voltage V_B. Calculate the small-signal output resistances of the current sources of *Figure 4(a)*, and *Figure 4(b)*, using the appropriate transistor data given below. You may assume that the current source connected to the emitter of Q1 (*Figure 4(a)*) and to the source of M1 (*Figure 4(b)*) has an incremental output resistance of 100 kΩ at a bias current of 1mA. Assume V_T, the transistor thermal voltage, is 26 mV at room temperature. [12]

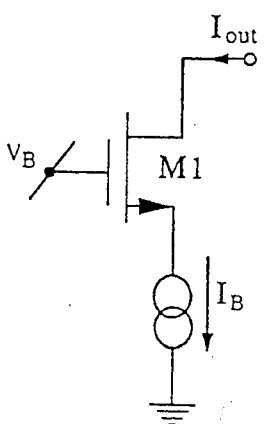
Finally, sketch typical circuits of a Widlar, Cascode and Wilson current mirror and give one advantage and disadvantage of each. Explain qualitatively how the action of negative feedback in the Wilson current-mirror increases output resistance. [6]

Transistor data:

BJT: $\beta = 100$ @ **1mA** **Ea = 100V**
MOSFET: $\lambda = 0.02$ **W/L = 10** $K_N = 20mA/V^2$



(a)



(b)

Figure 4

5. Show how the combination of a common-emitter and common-base amplifier helps to break the conflict between voltage gain and bandwidth in a single stage amplifier. [6]

Sketch the large signal voltage gain characteristic of a MOSFET common-source amplifier with active load. Describe the various regions of the curve, in particular, the region best suited for linear analogue amplification. [4]

Explain why the small signal voltage gain of the FET in saturation increases if the drain current is reduced. [2]

Sketch a suitable single-stage CMOS voltage amplifier which will give a bandwidth BW of

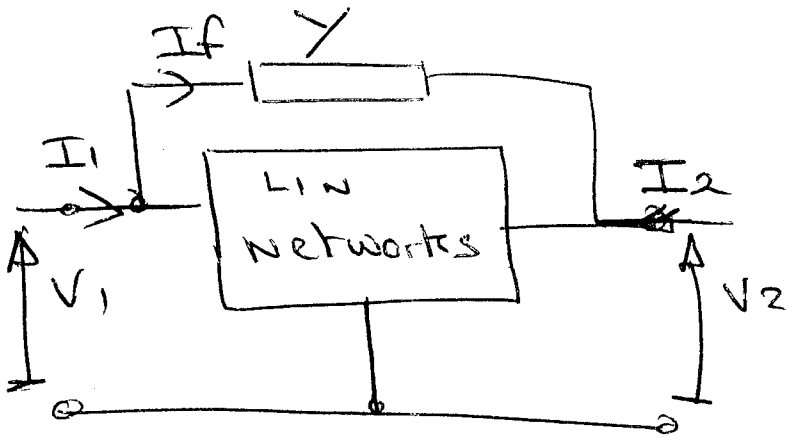
$$BW = [(g_{o1}g_{o2}/g_{m2}) + g_{o3}]/[2\pi C_L]$$

where go is device output conductance and C_L is the effective amplifier load capacitance. Assume all devices are operating in the high gain saturation region and the amplifiers bandwidth is dominated by the output of the amplifier. [3]

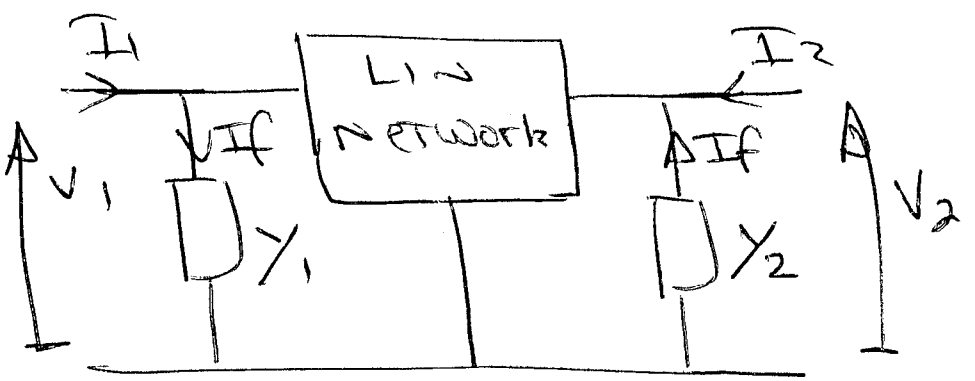
Finally, comment on the amplifiers phase margin and show how it is effected by a reduction in load capacitance C_L. [5]

2E Exam Solutions

1/.



Equivalent circuit.



— (3)

$I_f = Y_1 V_1 = -Y_2 V_2$

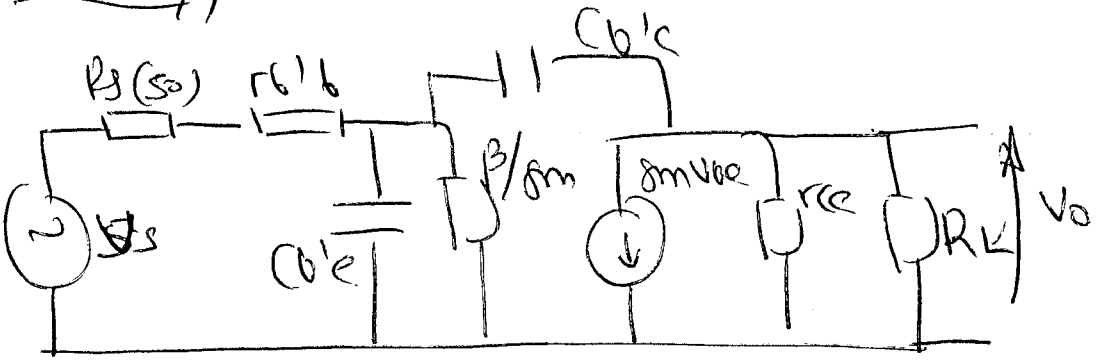
Eliminating I_f, $Y_1 V_1 = Y(V_1 - V_2)$

$\therefore Y_1 = Y(1 - V_2/V_1)$ $Y_1 = Y(1-A)$ —(1)

Similarly

$Y_2 = Y(1 - V_1/V_2)$ —(2)

1 and 2 confirm Millers theorem. — (3)



— (4)

To calculate $I_{CQ} = I_S \exp[V_{BE(ON)}/V_T]$
$= 1\,mA$

$\therefore g_m = (1/26)\,s$, $r_{ce} = \frac{100}{1}\,k\Omega$

$\beta/g_m \approx 2.6k$, $r_{b'b} = 50$

Bandwidth due to input

$f_{p1} = 1/2\pi R_{IN} C_{IN} \Rightarrow R_{IN} = (R_S + r_{bb'}) // \beta/g_m$
$= 100 // 2.6\,k\Omega \approx 96$

$C_{IN} = C_{b'e} + C_{b'c}(1+A)$
$\rightarrow 437\,pF$ — (4)

$A = V_o/V_{b'e} \approx g_m R_L'$, $R_L' = r_{ce} // R_L$
$= 6k // 100k$
$= 5.66k.$

$A = -217 \rightarrow$ Require $C_{b'e}$

from $f_T = g_m/2\pi(C_{b'e} + C_{b'c})$ — (4)

So $C_{b'e}$ can be estimated as 12.23pF

and so $C_{IN} = 449.6\,pF$

$\therefore$ **$f_{p1} = 3.69\,MHz.$** — (2)

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2/

$$A_V = -g_m / (g_{o1} + g_{o2})$$

$$g_m = 2\sqrt{\beta \cdot I_D}$$

$$(g_{o1} + g_{o2}) = (\lambda_1 + \lambda_2) I_D$$

$$\Rightarrow A_V = \frac{-2}{(\lambda_1 + \lambda_2)\sqrt{I_D}}\sqrt{\beta}$$

Since $I_D = \beta_2 (|V_{GS2}| - V_T)^2$

then $A_V = -\frac{2}{(\lambda_1 + \lambda_2)\sqrt{\frac{\beta_1}{\beta_2}}} \cdot \frac{1}{(|V_{GS}| - |V_T|)}$ — (10)

Since $V_{bias} = 2V$, $|V_{SS}| = 3V$

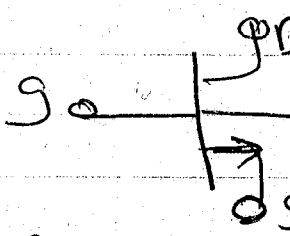
$$\Rightarrow (V_{SS} - V_T) = 1V$$

$$\therefore A_V = \frac{-2}{0.03}\sqrt{2\frac{W_1}{W_2}}$$ Assuming equal L

$$= -94.3 \left(\frac{W_1}{W_2}\right)^{1/2}$$ — (5)

Body effect

The MOSFET is a four terminal device



Substrate / Body of Device

Parasitic junctions (PN) exist between Body and Channel and so substrate should be connected more negative than source in N-channel and more positive than source in P-channel.

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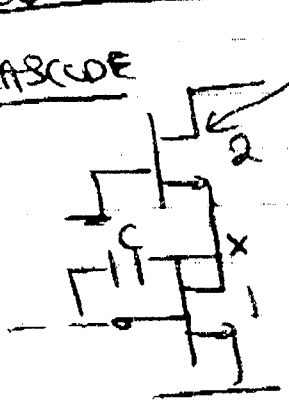
V_{BS} voltage is generated in V_T and is refered to as the Body effect.

$$V_T = V_{T0} + \gamma\left[\sqrt{-V_{BS} + 2\phi_F} - \sqrt{2\phi_F}\right] \quad - (5)$$

Question 3

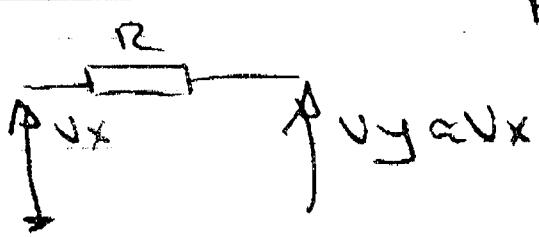
CASCODE



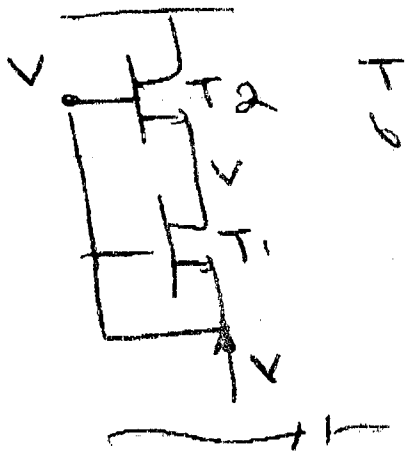
Cascoding is a technique which uses a common-base / common-gate transistor to keep the collector / drain of a common-emitter / common-source transistor at an 'almost' virtual constant voltage x

The input miller capacitance is reduced from $C_{IN} = (1 + g_m r_{CE})C$ to $C_{IN} \approx 2C$ where $g_m r_{CE}$ is the open-circuit voltage gain of T1 and the assumption is that $g_{m1} = g_{m2}$. The output resistance of the cascoded device also remains since the drain current of T1 stays 'almost' constant when variation in output voltage. — (3)

Bootstrapping

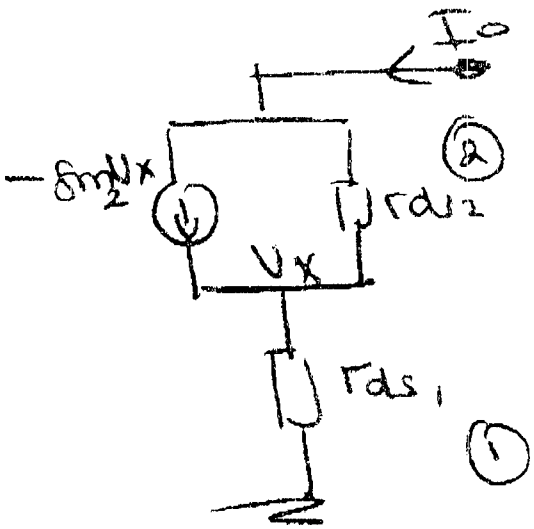


Analogue bootstrapping is a technique used to ensure that both ends of a device are held at the same a.c potential resulting in theoretically zero 'ac' current through the device and thus very high output resistance. The technique is usually used to create high quality current sources — (3)



T2 Bootstrapes T1 by ensuring that the source and drain of T1 are held at the same potential

Consider the bottom half of Figure 3



Can show that

$\frac{V_o}{I_o}$ = Rout Bottom

$= g_{m2} r_{ds2} r_{ds1}$

$= g_{m2} / (g_{o1} \cdot g_{o2})$

Then can be derived

From $V_x = I_o r_{ds1}$ - (1)

$I_o = -g_{m2} V_x + \frac{(V_o - V_x)}{r_{ds1}}$ - (2)

Subs (1) into (2) gives the above result.

Since the top-half will give a similar result, then it can similarly be shown that

Rout TOP = $g_{m3} / g_{o3} g_{o4}$

In terms of G_{out}

When $G_{out1} = G_{OT} + G_{OB}$

$$= \left[\frac{g_{01}g_{02}}{g_{m2}} + \frac{g_{03}g_{04}}{g_{m3}}\right]$$

Assume $V_{IN} = 0$, drawing output. -(10)

Output swing

$V_{SD(4)} = (V_{SG} - |V_t|)_{(min)}$

$V_{DD} = (4 - 2) = 2V$

Source of $Q_3 = 8V$

$\therefore V_{SG(3)} = 3V$

$\therefore V_{SD(3)} = (3 - 2) = 1V$

Minimum voltage across Q_3 and Q_4 = 3V $\therefore$ maximum swing = $(10 - 3) = \underline{7 \text{ volts}}$

Assume equal size devices. -(4)

Total 20/20

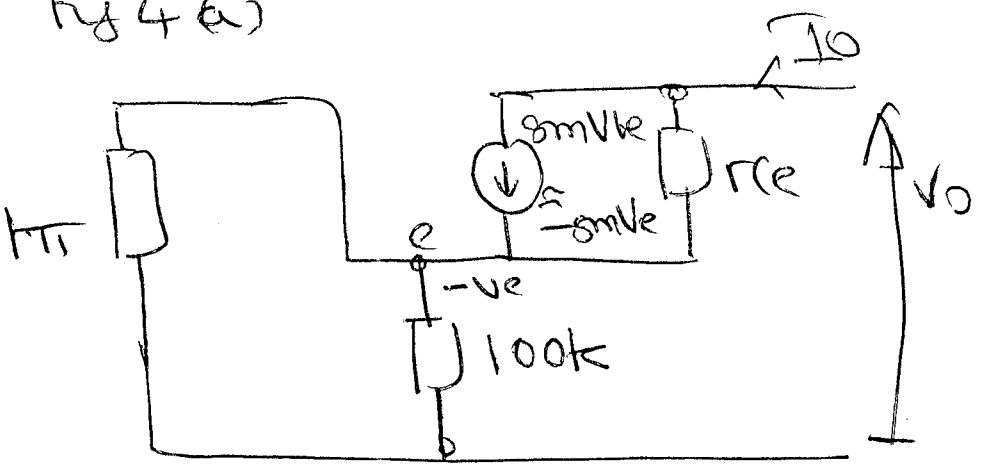
4/. Main reason for creating current sources and current sinks

- High gain amplifier stages
- Precision current mirrors
- High resistance with minimal silicon
- Large circuit with low power supply voltage.

(2)

OUTPUT RESISTANCE

Fig 4(a)



$$Ve = Io[100k // r\pi]$$

$$Vo = (Io + gmVe)\,rce + Ve$$

$$\simeq Io\,rce + Ve\,(gm\,rce + 1)$$

$$\simeq Io\,[rce + gm\,rce\,(100k // r\pi)]$$

$$\simeq Io\,[gm\,rce\,(100k // r\pi)]$$

$$\simeq Vo/Io \sim Rout = gm\,rce\,(100k // r\pi)$$

$$r\pi \simeq \beta re \simeq \beta/gm \Rightarrow gm\,Ic/Vt$$

$$= 0.038s$$

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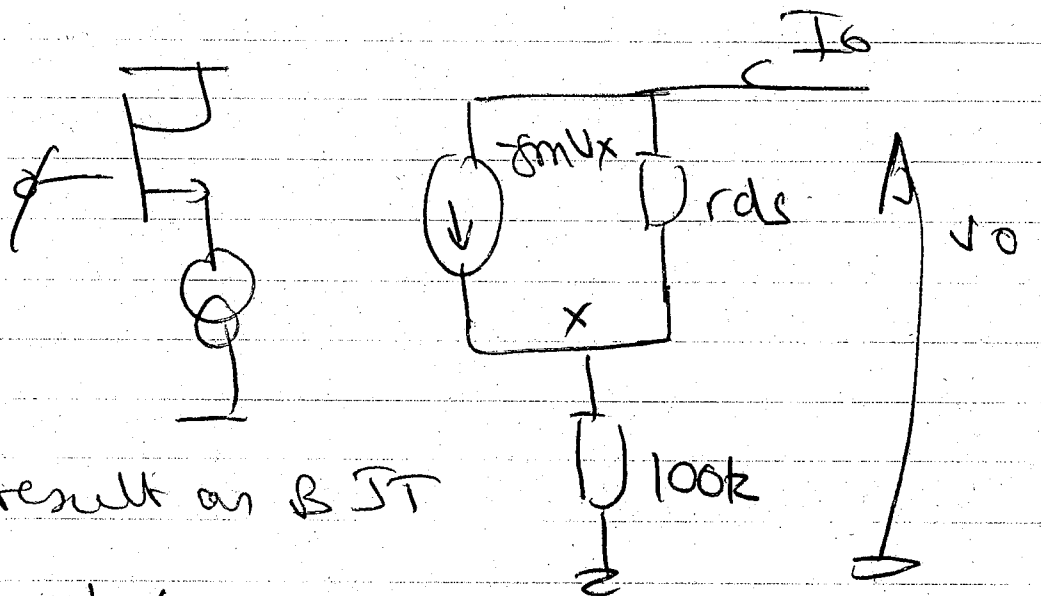
- $r_\pi = 2.6315 k\Omega$

- $r_e \approx (Ea/1mA) \approx 108 k\Omega$

- $R_{out} = 9.73 M\Omega$. — (6)

4(b)



same result as BJT

$R_{out} = V_o / I_o$

$= g_m r_{ds} (100k)$, since no bias

$r_\pi \Rightarrow \infty$

$R_{out} = [g_m / (-I_D)](100k)$

$g_m = 2\sqrt{\beta I_D} \Rightarrow \beta = \frac{k_n W}{2L} = 100 \times 10^{-6} A/V$

$\approx 6.32 \times 10^{-4}$

$R_{out} = 3.162 M\Omega$ — (6)

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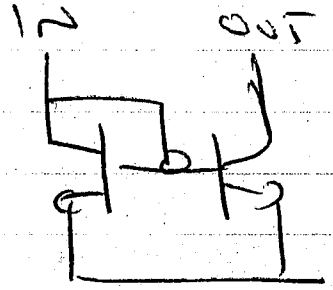
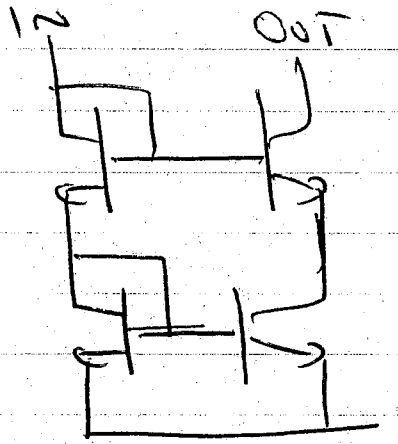


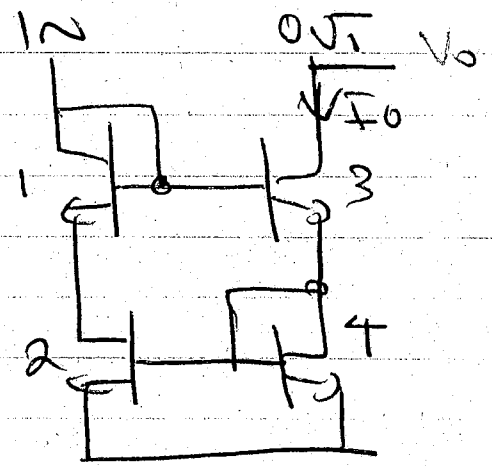
High speed
low accuray

CASCOOR



High output R
reduced swing
for de Beta
error

WILSON



small β error
high output
R.

— (3)

Wilson

High output R through negative feedback. Change in output Vo will change Io Increasing Vbe 4 and Vbe2 (negative feedback) Since I_{in} constant, I_{b3} reduces, base voltage of Q3 reduces and $I_{C3} = I_o$ reduces. ∴ current held almost constant independent of output voltage.

— (3)

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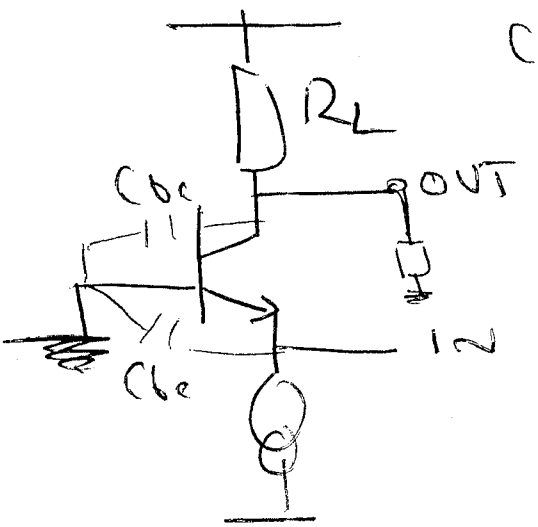
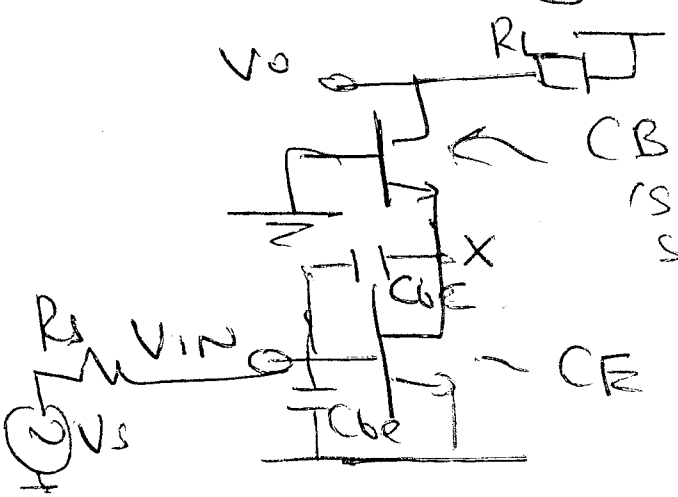


CB amplifier

— (3)

The CB amplifier when used as a current-follower (current in and out) will work upto the f_T of the transistor. No Miller capacitance across gain stage If RL sufficiently high then Bandwidth is dominated by $1/g_m$ and [Cbe + Cbc]



CB stage holds X node (still) keeps voltage swing low. Cbc of CE only sees ≈ 2 VIN (assuming ($g_{m1} = g_{m2}$).

Thus Miller gain ≈ 2 and is constant.

$A \approx g_m R_L$ → set independently of

Bandwidth determined by [2Cbc + Cbe]

(3)

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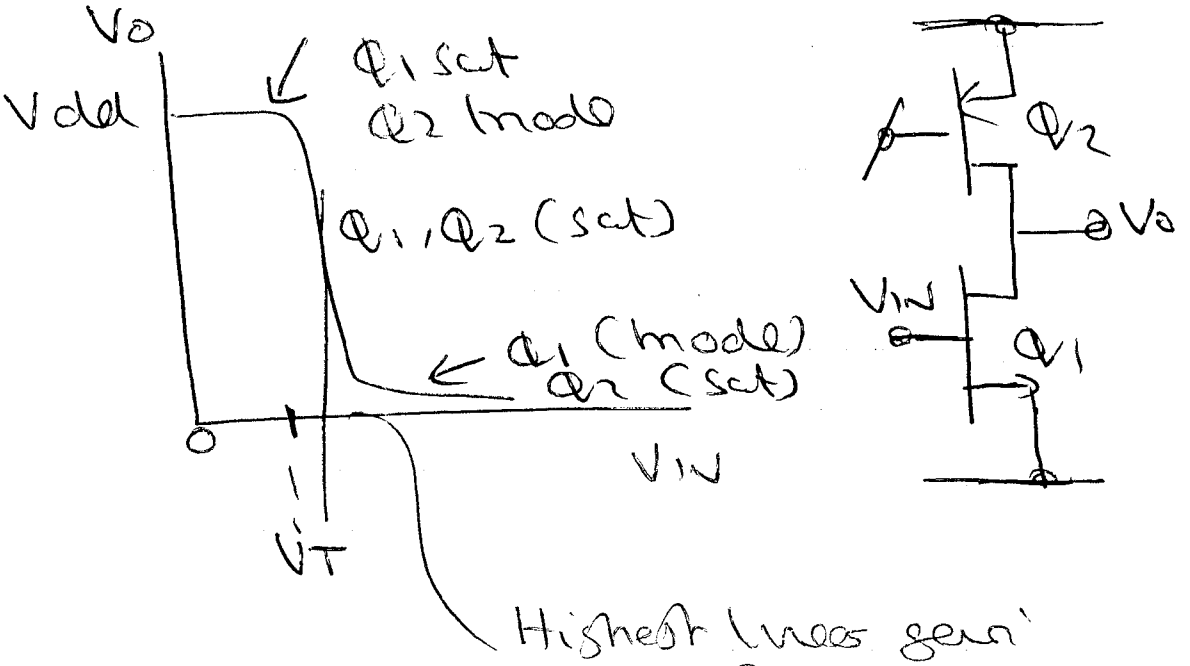
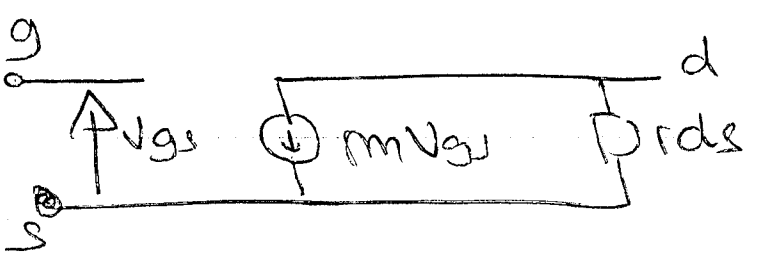


Highest linear gain region. Region for small signal voltage gain.

(4)



$A_V = g_m r_{ds}$

$g_m = 2\sqrt{\beta I_D}$

$g_o = 1/r_{ds} = \lambda I_D$

} I_D is current drawn current.

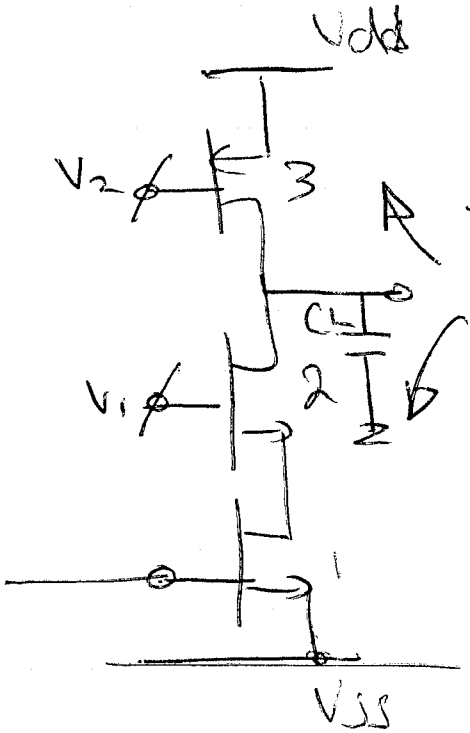
$$g_m/g_o = \frac{2}{\lambda}\sqrt{\beta/I_D} \simeq A$$

(2)

eg g_m proportional to $\sqrt{I_D}$

g_o " " I_D

g_m/g_o " " $1/\sqrt{I_D}$.

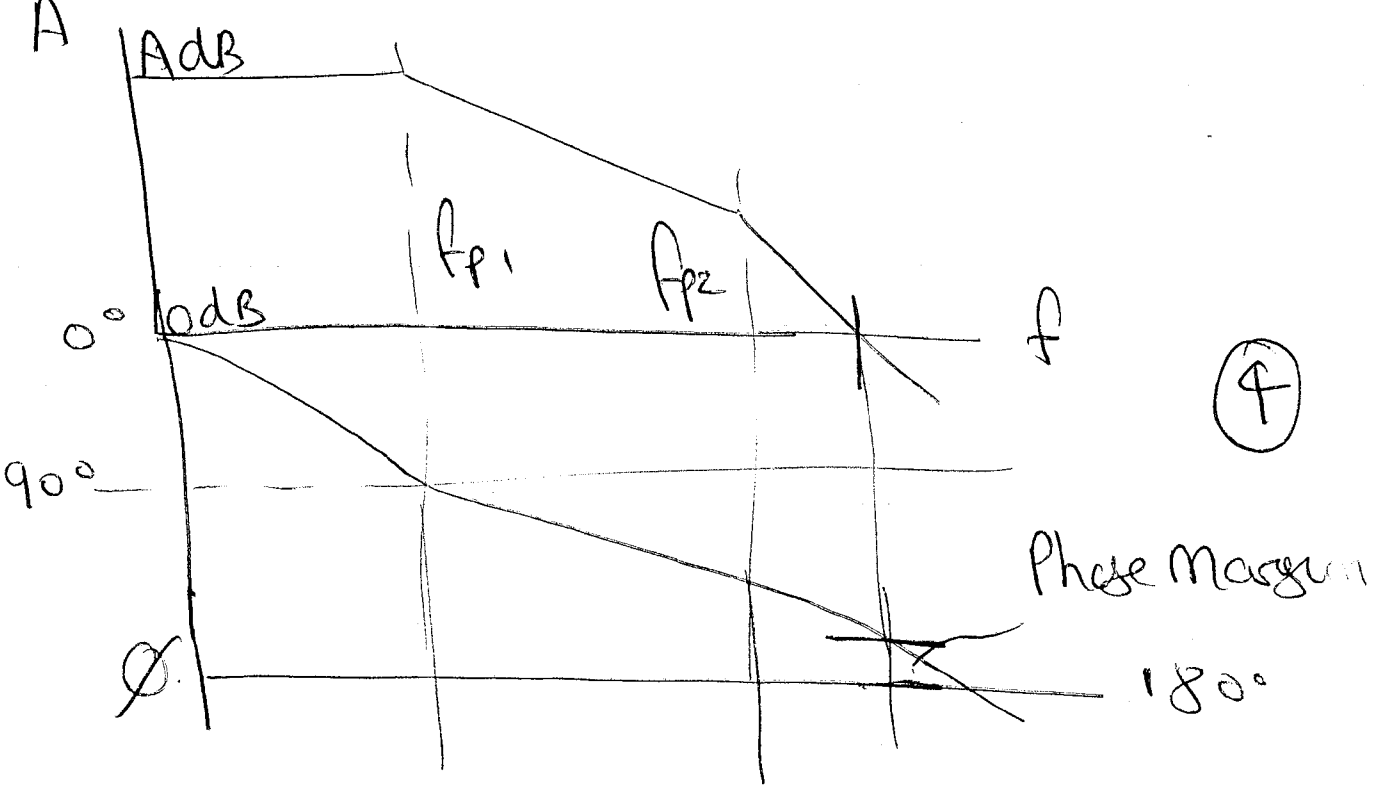


$$\Rightarrow G_0 = g_{03} + \frac{g_{01} g_{02}}{g_{m2}}$$

$\frac{g_{01} g_{02}}{g_{m2}}$

(4)

Bandwidth dominated by output pole. f_{p1}



(4)

As C_L is reduced, f_{p1} increases and approaches f_{p2} reducing phase difference between 180° and unity gain phase