2013 Electronic and Electrical Fundamentals

Intermediate 2

Finalised Marking Instructions

Part One: General Marking Principles for: Electronic and Electrical Fundamentals Intermediate 2

This information is provided to help you understand the general principles you must apply when marking candidate responses to questions in this Paper. These principles must be read in conjunction with the specific Marking Instructions for each question.

(a) Marks for each candidate response must always be assigned in line with these general marking principles and the specific Marking Instructions for the relevant question. If a specific candidate response does not seem to be covered by either the principles or detailed Marking Instructions, and you are uncertain how to assess it, you must seek guidance from your Team Leader/Principal Assessor.

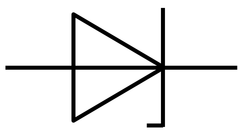
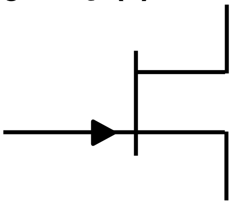
(b) Marking should always be positive ie, marks should be awarded for what is correct and not deducted for errors or omissions.

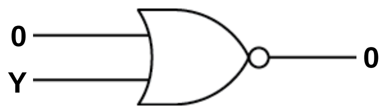
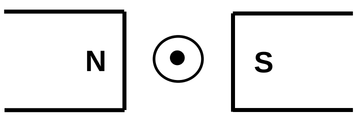
GENERAL MARKING ADVICE: Electronic and Electrical Fundamentals Intermediate 2

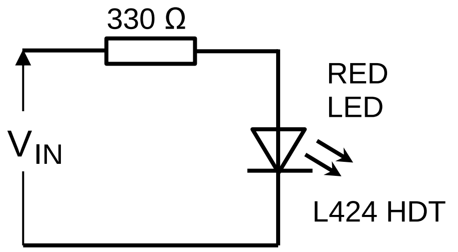
The marking schemes are written to assist in determining the “minimal acceptable answer” rather than listing every possible correct and incorrect answer. The following notes are offered to support Markers in making judgements on candidates’ evidence, and apply to marking both end of unit assessments and course assessments.

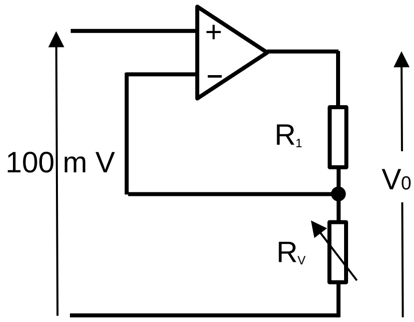
Part Two: Marking Instructions for each Question

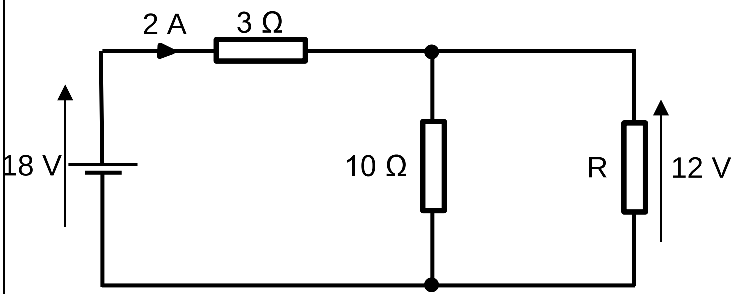
Section A

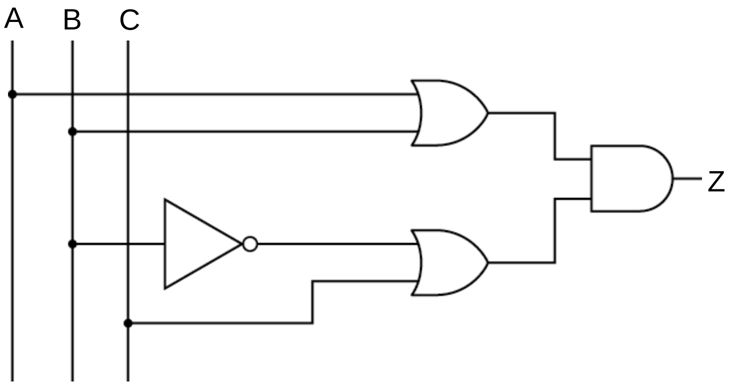
Question			Expected Answer/s	Max Mark	Additional Guidance
1			**Convert the following numbers.**		
	a		**Binary to Decimal** $\mathbf{11101001_2}$ 233_{10}	**2**	
1	**b**		**Hexadecimal to Binary** $\mathbf{E4_{16}}$ 11100100_2	**2**	
1	**c**		**Decimal to Hexadecimal** $\mathbf{215_{10}}$ $D7_{16}$	**2**	
2			**Identify the circuit symbols shown in Figure Q2(*a*) and Figure Q2(*b*)**		
	a		**Figure Q2(*a*)**  Zener diode	**2**	
2	**b**		**Figure Q2(*b*)**  FET	**2**	

Question			Expected Answer/s	Max Mark	Additional Guidance
3			**Determine the logic input X and Y for the gates shown in Figure Q3(*a*) and Figure Q3(*b*) respectively.**		
	a		**Figure Q3(*a*)**  X = 1	1	
3	b		**Figure Q3(*b*)**  Y = 1	1	
4			**Figure Q4 shows a current carrying conductor placed between magnetic poles. The magnetic flux density is 0·2 Tesla. The conductor experiences a force of 1·2 N when the current is 15 A.** **Figure Q4**  		
	a		**Determine the length of conductor within the magnetic field.** $l = \frac{F}{Bi} = \frac{1\cdot 2}{0\cdot 2\times 15} = 0\cdot 4$ m	2	
4	b		**State what happens to the force when the current direction is reversed.** Reverses or stays the same size	1	

Question			Expected Answer/s	Max Mark	Additional Guidance
5			**Referring to Figure Q5, and using the supplied datasheet:** **Figure Q5**  		
	a		**state the purpose of the series resistor** The series resistor limits the current to protect the LED	1	
5	b		**state the maximum forward current the diode can handle** $I_F(max) = 25$ mA	1	
5	c		**state the typical forward voltage drop** $V_F(typ) = 2$ V	1	
5	d		**determine the maximum value of input voltage that can be safely applied.** $V_{in}(max) = (0{\cdot}025 \times 330) + 2 = 10{\cdot}25$ V	2	
6			**A generator produces a sinusoidal current represented by the equation** $i = 12\sin\theta$ amperes **Determine:**		
	a		**the maximum value of the current** 12 A	1	

Question			Expected Answer/s	Max Mark	Additional Guidance
6	b		**the r.m.s. value of the current** Irms = 0·707 × 12 = 8·48 A	**1**	
6	c		**the average value of the current** I ave = 0·637 × 12 = 7·64 A	**1**	
6	d		**the instantaneous value of the current when $\theta = 30°$** i = 12sin30 = 12 × 0·5 = 6 A	**2**	
7			**With reference to the circuit shown in Figure Q7, in which resistor R1 is 10 kΩ and** R_v **can be varied between 5 kΩ and 15 kΩ:** **Figure Q7** 		
	a		**name the circuit configuration** non inverting amplifier	**1**	
7	b		**determine the output voltage when** R_v **is set to 10 kΩ** $\text{gain} = \frac{R1 + R2}{R2} = \frac{10k + 10k}{10k} = 2$ Vout = 100 mV × 2 = 200 mV	**2**	

Question			Expected Answer/s	Max Mark	Additional Guidance
7	c		**determine the maximum possible output voltage when the input is 100 mV** $\text{max gain} = \dfrac{R1 + R2}{R2} = \dfrac{10k + 5k}{5k} = 3$ Vout = 100 mV × 3 = 300 mV	3	
7	d		**determine the minimum possible output voltage when the input is 100 mV** $\text{min gain} = \dfrac{R1 + R2}{R2} = \dfrac{10k + 15k}{15k} = 1{\cdot}67$ Vout = 100 mV × 1·67 = 167 mV	3	
8			**With reference to the circuit shown in Figure Q8:** **Figure Q8**  		
	a		**determine the voltage across the 3 Ω resistor** $V_{3\Omega} = I_s \times R = 2 \times 3 = 6$ V	1	
8	b		**determine the current through the 10 Ω resistor** $I_{10\Omega} = \dfrac{V_p}{10} = \dfrac{12}{10} = 1{\cdot}2\ \text{A}$	2	
8	c		**determine the value of resistor R.** $I_R = I_S - I_{10\Omega}$ $I_R = 2 - 1{\cdot}2 = 0{\cdot}8$ A $R = \dfrac{V_p}{I_R} = \dfrac{12}{0{\cdot}8} = 15\ \Omega$	3	

<table>
<tr><th colspan="3">Question</th><th>Expected Answer/s</th><th>Max Mark</th><th>Additional Guidance</th></tr>
<tr><td>8</td><td>d</td><td></td><td>A fault condition causes the 10 Ω resistor to be open circuit. Determine the new value of supply current.
$R_T = 3 + 15 = 18\ \Omega$
$I_S = \frac{V_S}{R_T} = \frac{18}{18} = 1\ A$</td><td>2</td><td></td></tr>
<tr><td>9</td><td>
a</td><td></td><td>For the circuit shown in Figure Q9:
Figure Q9


Determine the Boolean expression for output Z
$Z = (A + B).(\overline{B} + C)$</td><td>
2</td><td></td></tr>
<tr><td>9</td><td>b
c</td><td></td><td>Draw the truth table for the circuit
Determine the circuit output Z when a faulty condition causes the output of the invertor to be permanently low (logic 0)</td><td>4
2</td><td></td></tr>
<tr><td colspan="6">
<table>
<tr><td></td><td></td><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td>c.</td></tr>
<tr><td>A</td><td>B</td><td>C</td><td>A + B</td><td>$\overline{B}$</td><td>$\overline{B}$ + C</td><td>(A + B).($\overline{B}$ + C)</td><td>Fault</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
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</td></tr>
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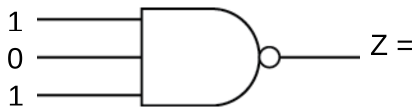
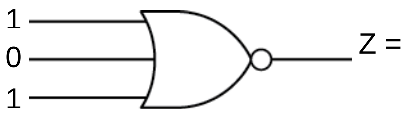
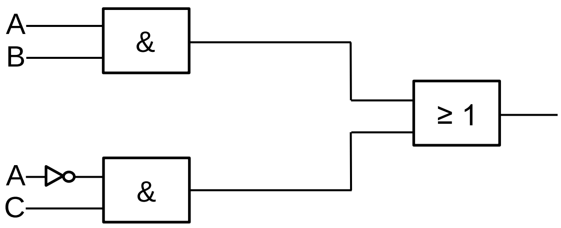
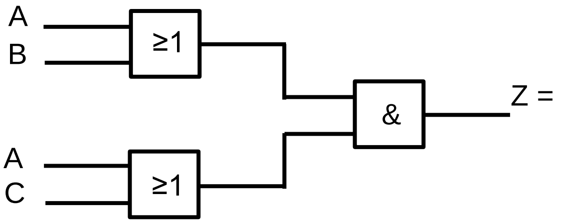
Section B

Question			Expected Answer/s	Max Mark	Additional Guidance
10	a	i	**Attempt any TWO questions in this section (50 marks). Each question is worth 25 marks.** **State the logic output for the logic gates shown in Figure Q10(*a*)(i) and Figure Q10(*a*)(ii).** **Figure Q10(*a*)(i)**  Z = 1	2	
10	a	ii	**Figure Q10 (*a*)(ii)**  Z = 0	2	
10	b	i	**Add the following binary numbers.** **$0101_2 + 0101_2$** 1010_2	2	
10	b	ii	**$0010_2 + 0101_2$** 0111_2	2	
10	c		**Draw the logic circuit for the expression** Z = A.B + $\bar{A}$ .C	3	
					Ans I symbols and other logic combinations are acceptable.

Question			Expected Answer/s	Max Mark	Additional Guidance
10	d		**Determine the logic expression for the logic circuit shown in Figure Q10(*d*).**	3	

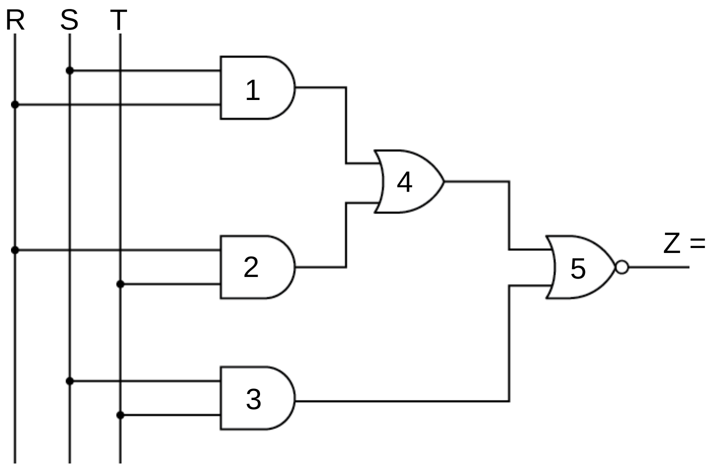
Figure Q10(*d*)



Z = (A + B).(A + C)

Question			Expected Answer/s	Max Mark	Additional Guidance
10	e		**Figure Q10(*e*)(i) shows a logic circuit.**		

Figure Q10(*e*)(i)

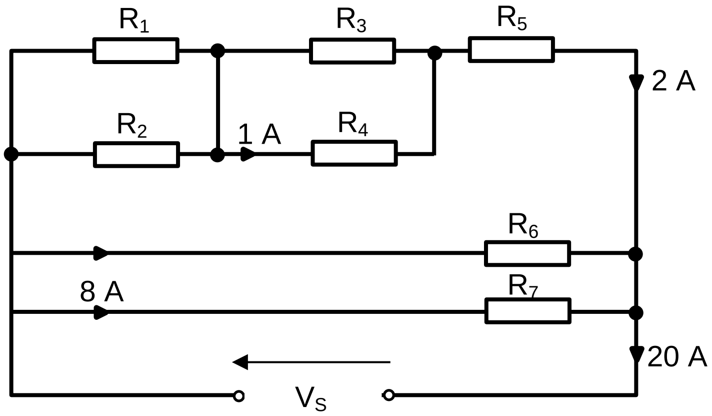


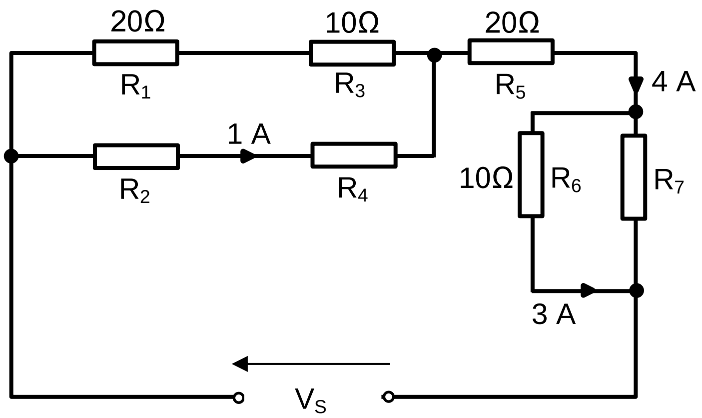
Question			Expected Answer/s	Max Mark	Additional Guidance
		i	**Determine the logic expression for the circuit.**	3	

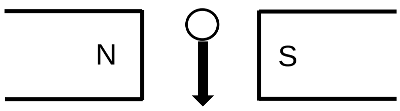
$Z = \overline{(R.S + R.T) + S.T}$

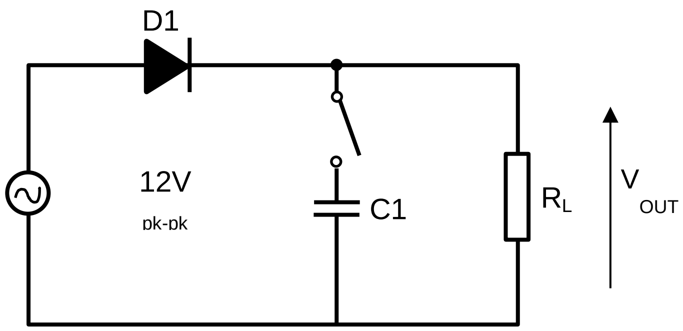
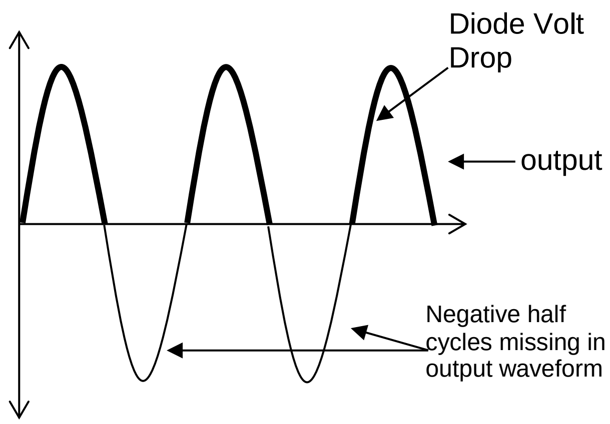
Question			Expected Answer/s	Max Mark	Additional Guidance
10	e	ii	**Draw the truth table for the circuit.**	4	Intermediate columns are not necessarily required to be shown in the solution.

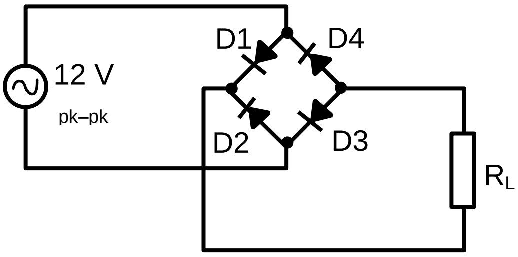
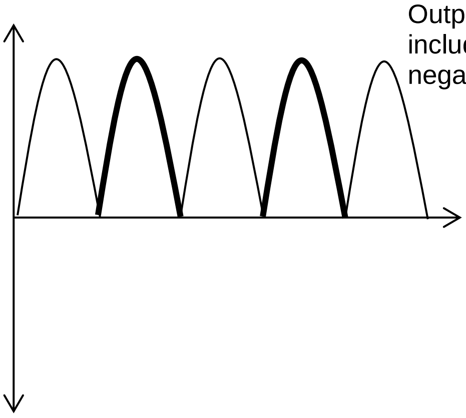
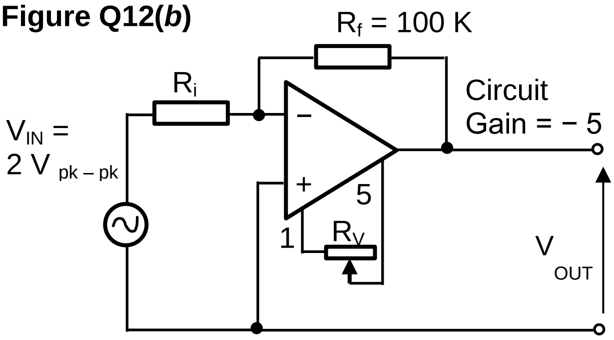
R	S	T	R.S	R.T	R.S+R.T	S.T	(R.S+R.T)+S.T	**Z**
0	0	0	0	0	0	0	0	**1**
0	0	1	0	0	0	0	0	**1**
0	1	0	0	0	0	0	0	**1**
0	1	1	0	0	0	1	1	**0**
1	0	0	0	0	0	0	0	**1**
1	0	1	0	1	1	0	1	**0**
1	1	0	1	0	1	0	1	**0**
1	1	1	1	1	1	1	1	**0**

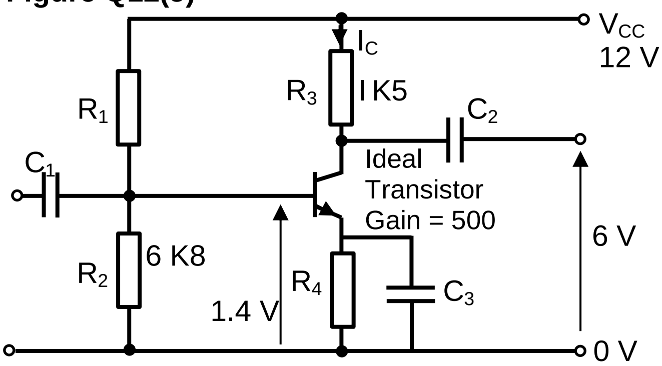
Question			Expected Answer/s	Max Mark	Additional Guidance
10	e	iii	**The circuit shown in Figure Q10(*e*)(i) has developed a fault, and upon testing the outputs shown in the truth table Figure Q10(*e*)(iii) were obtained. Explain which gate (input or output) is at fault and state the nature of the fault.** **Figure Q10(*e*)(i)** R S T Z: 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 0 1 0 0 1 1 0 1 1 1 1 0 0 1 1 1 0 1011 The only output that is wrong is for input 101 (line 6), as the final gate (5) is a nor gate this means that both the inputs at this time must both be zeros (0). The input from gate 3 (lines 4 and 8) appear to be okay then the fault must lie with the input from gate 4, however as the input to gate 4 from gate 1 (line 7) is correct then the fault must be due to the input from gate 2. The fault may be that the output from gate 2 is always 0 or that the input to gate 4, from gate 2 is tied to zero 0.	4	
11	a		**For the circuit shown in Figure Q11(*a*), determine:** **Figure Q11(*a*)** 		
		i	**the current flowing in R_3** By KCL current in $R_3 = I(R_5) – I(R_4) = 2 – 1 = 1$ A	2	

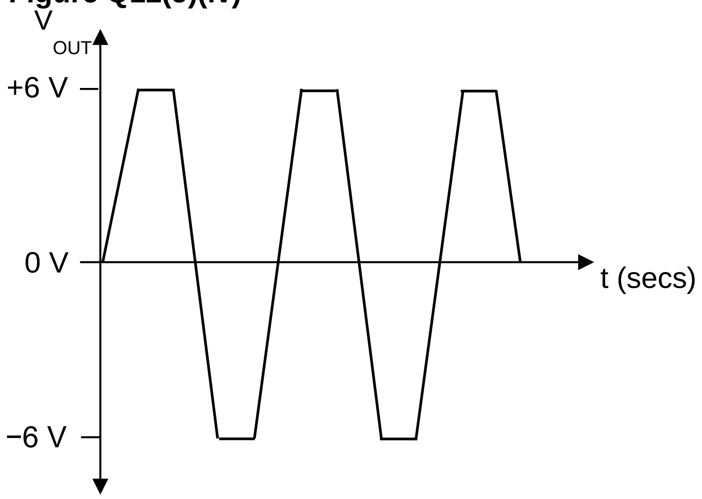
Question			Expected Answer/s	Max Mark	Additional Guidance
11	**a**	**ii**	**the current flowing in R_6** By KCL $I(R_6) = Is - I(R_7) - I(R_5) = 20 - 8 - 2 = 10$ A	**2**	
11	**b**		**For the circuit shown in Figure Q11(*b*), determine:**		
		i	**Figure Q11(*b*)**  **the voltage drop across R_7** Voltage drop across R_7 = voltage drop across R_6 $= I \times R_6 = 3 \times 10 = 30$ V	**2** **2**	
11	**b**	**ii**	**the supply voltage** By KVL the supply voltage = the sums of the voltage drops around the circuit $V_S = I_1 \times (R_1 + R_2) + I_5 \times R_5 + I_6 \times R_6$ $V_S = (3 \times 30) + (4 \times 20) + 30 = 90 + 80 + 30 = 200$ V The application of KCL is also required in this question.	**3**	
11	**b**	**iii**	**the power dissipated in R_7** $P = V \times I = 30 \times 1 = 30$ W	**2**	
11	**b**	**iv**	**the energy consumed in 3 hours by the branch containing R_2 & R_4** $W = V \times I \times t = 90 \times 1 \times (3 \times 60 \times 60) = 972$ kJ	**3**	

Question			Expected Answer/s	Max Mark	Additional Guidance
11	c	 i	**A variable speed, 10 kW generator produces an output voltage of 120 V, has a flux density of 40 milliTesla, and a conductor length of 25 m. Calculate:** **the speed of the generator;** E = B × L × v hence $v = \frac{E}{(B \times L)}$ $v = \frac{120}{(40 \times 10^{-3} \times 25)} = \frac{120}{0 \cdot 1} = 120\ ms^{-1}$	 3	
11	c	ii	**the speed of the generator when the output voltage is 200 V;** $v = \frac{200}{0 \cdot 1} = 200\ ms^{-1}$	2	
11	c	iii	**the maximum current the generator can supply when the output is 200 V.** P = V × I hence $I = \frac{P}{V} = \frac{10000}{200} = 50\ A$	2	
11	d	 i	**A conductor is forced to move downwards within a magnetic field, as shown in Figure Q11(*d*).** **Figure Q11(*d*)**  **State the formula used to calculate the current in the conductor.** F = B × L × I hence $I = \frac{F}{(B \times L)}$	 1	

Question			Expected Answer/s	Max Mark	Additional Guidance
11	d	ii	**Explain how the direction of the current can be determined.** The direction of the current can be determined by using Flemings Right Hand rule, where the direction of motion (force) is indicated by the thuMb, the direction of the magnetic field is indicated by the First finger and the direction of the current is indicated by the seCond finger. (Alternative answers are also acceptable)	3	
12	a		**For the circuits shown in Figures Q12(*a*)(i) and (ii) the input voltage is 12 V_{pk-pk},50 Hz in each circuit.**		
	i		**Assuming that the switch remains open, sketch the input and output waveforms for the circuit shown in Figure 12(*a*)(i), clearly indicating the differences between the input waveform and the output waveform.** **Figure 12(*a*)(i)** 	3	
					A 0.6V or 0.7V diode volt drop is acceptable

Question			Expected Answer/s	Max Mark	Additional Guidance
12	a	ii	**Sketch the output waveform for the circuit shown in Figure 12(*a*)(ii), clearly indicating the differences between the new output waveform and the output waveform of Figure Q12(*a*)(i).** **Figure 12(*a*)(ii)** 	3	
					
12	b		**For the circuit shown in Figure Q12(*b*):** **Figure Q12(*b*)** 		
		i	**state the circuit configuration** Inverting amplifier	1	

Question			Expected Answer/s	Max Mark	Additional Guidance
12	b	ii	**determine the output voltage** $V_{OUT} = V_{IN} \times \text{Gain} = 2 \times -5 = 10\ V_{pk-pk}$	2	
12	b	iii	**determine the value of R_i** $\text{Gain} = \frac{-Rf}{Ri}$ hence $Ri = \frac{-Rf}{gain} = \frac{-100}{-5} = 20\ K$	2	
12	b	iv	**explain the purpose of R_v** The purpose of R_v is to adjust the output of the amplifier to zero when the input is zero. Offset Null adjustment.	2	
12	c	i	**Identify the circuit shown in Figure Q12(*c*).** **Figure Q12(*c*)**  Common Emitter Amplifier	1 1	
12	c	ii	**With reference to Figure Q12(*c*), identify the purpose of each of the following components: R_1 & R_2, C_2 & C_3.** R_1 & R_2 - Bias resistors C_2 - Coupling capacitors C_3 - Emitter bypass capacitor	4	
12	c	iii	**Calculate the output voltage for the circuit shown in Figure Q12(*c*) when the input voltage is 20 mV_{pk-pk}.** $V_{OUT} = \text{gain} \times V_{IN} = 500 \times 20\ mV = 10\ V_{pk-pk}$	2	

Question			Expected Answer/s	Max Mark	Additional Guidance
12	**c**	**iv**	**When the input voltage is increased to 40 mV$_{pk-pk}$ the output waveform is as shown in Figure Q12(*c*)(iv).** **Figure Q12(*c*)(iv)**  **Explain why the shape of the waveform is non-sinusoidal.** The waveform has been clipped at the supply voltage as the amplifier is being over-driven (the gain is too high for the input)	**3**	
12	**c**	**v**	**Suggest two ways of preventing this.** Reduce the gain of the amplifier Reduce the input voltage Increase the supply voltage	**2**	

[END OF MARKING INSTRUCTIONS]