2012 Electronic and Electrical Fundamentals

Intermediate 2

Finalised Marking Instructions

Section A

Attempt all the questions in this section (50 marks)

1. Convert the following numbers.

(a) 21_{10} Decimal to Binary

(b) $B9_{16}$ Hexadecimal to Binary

(c) 10011001_2 Binary to Decimal

Answers

(a) 000010101_2 **2**

(b) 10111001_2 **2**

(c) 153_{10} **2**

(6)

2. With reference to Figures Q2*(a)* and Q2*(b)* name the components shown and state **one** application for each.

(a)

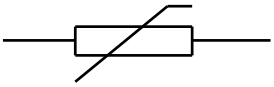


Figure Q2(a)

(b)

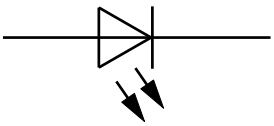


Figure Q2(b)

Answers

(a) Component: Preset resistor **1**
Application: Voltage control/setting **1**

(b) Component: LED (Light Emitting Diode) **1**
Application: Illumination, Signal information (on/off) **1**

(4)

3. In an experiment to plot the magnetic field between two magnetic poles, a brass ring and an iron ring were placed in the field and the field pattern recorded. The results are shown in Figures Q3*(a)* and Q3*(b)*.

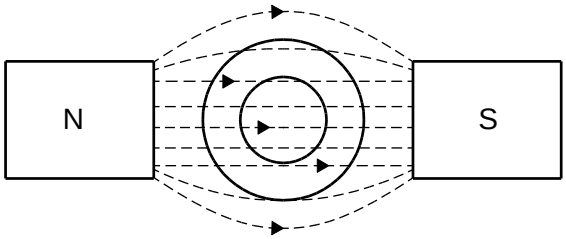


Figure Q3*(a)*

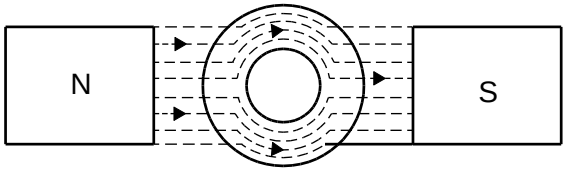


Figure Q3*(b)*

(a) State which result shows the experiment with the brass ring and justify your answer.

(b) A 500 mm conductor carrying a current of 10 A is placed in a magnetic field of 5 T. Determine the force acting upon the conductor.

Answers

(a) Result Figure Q3(*a*) shows the experiment with the brass ring. **1**

The lines of magnetic flux are not affected by the brass ring while in Figure Q3(*b*) the lines are concentrated in the iron ring. **3**

(b) $F = Bli = 5 \times 0{\cdot}5 \times 10 = 25$ N **3**

(7)

Marks

4.

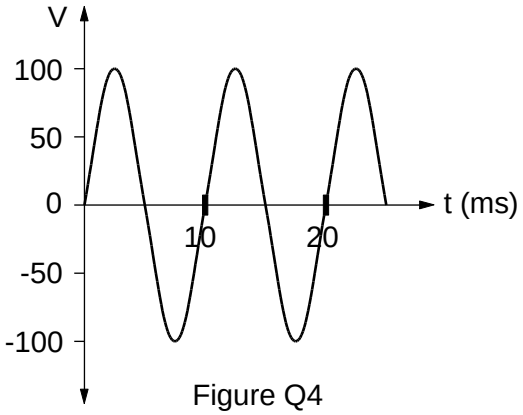


Figure Q4

The waveform shown in Figure Q4 was obtained from a display instrument.

Determine the following.

(*a*) The peak to peak value of the waveform.

(*b*) The r.m.s. value of the waveform.

(c) The period of the waveform.

Answers

(a) 200 V pk-pk **1**

(b) r.m.s. = Vpk $\times$ 0·707 = 70·7 V **2**

(c) Period = 10ms **1**

(4)

5. One possible circuit configuration using an operational amplifier is shown in Figure Q5. The supply voltages are not shown.

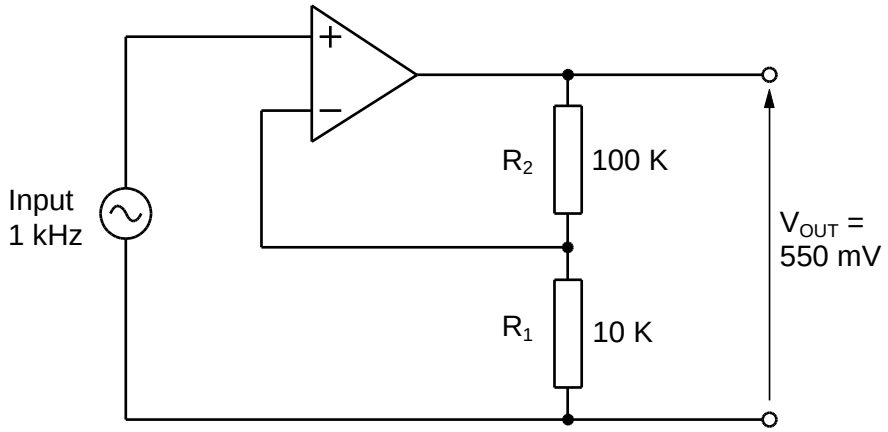


Figure Q5

(a) Name the circuit configuration.

(b) Calculate the gain of the circuit.

(c) Calculate the input voltage to the circuit.

Answers

(a) Non Inverting Amplifier **1**

(b) Gain Av = $\frac{(R_1 + R_2)}{R_1} = \frac{(10k + 100k)}{10k} = 11$ **2**

(c) Gain Av = $\frac{V_{out}}{V_{in}}$ therefore

$V_{in} = \frac{V_{out}}{gain} = \frac{550}{11} = 50mV$ **3**

(6)

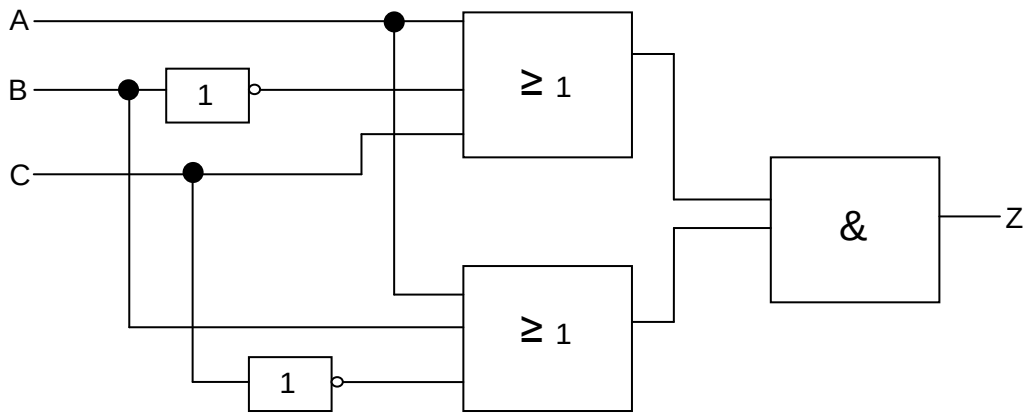
6. Draw using BS symbols, the logic diagrams for the following expressions.

(a) $Z = (A + \overline{B} + C) \cdot (A + B + \overline{C})$

(b) $Z = \overline{(\overline{A} + \overline{B} + C) \cdot (A + \overline{B} + \overline{C})}$

Answers

(a)



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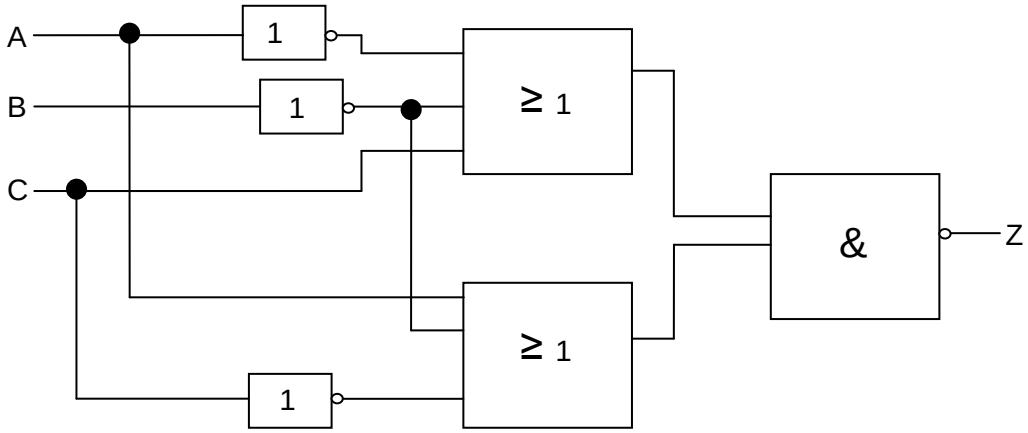
(b)



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(6)

7. A diode is connected as shown in Figure Q7. Using the information provided, and assuming the volt drop across the diode is 0·7 V:

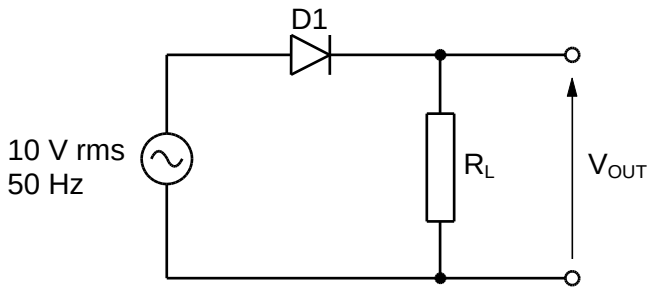


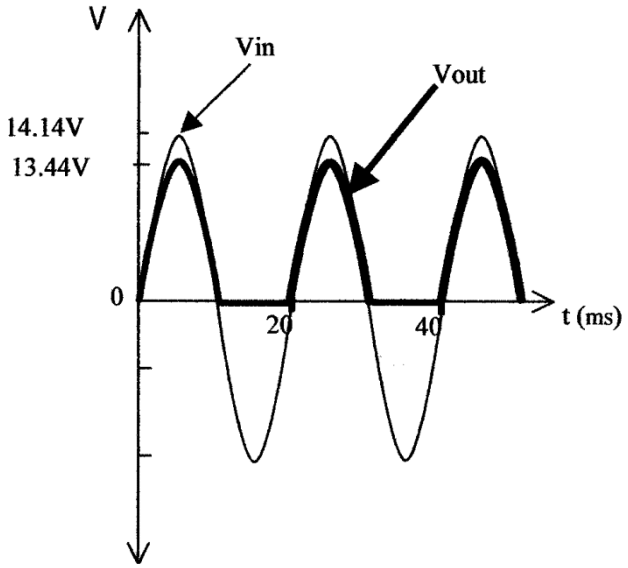
Figure Q7

(a) Sketch the input and output voltage waveforms;

(b) Explain the difference between the two waveforms.

Answers

(a)



3

(b) The input waveform is 14·14 V peak and the output waveform is only the positive half cycles, less the forward diode volt drop of 0·7 V, during the negative half cycle of the input waveform the diode is blocking and no voltage appears across the load. **3**

(6)

8. The circuit shown in Figure Q8 is a common emitter amplifier.

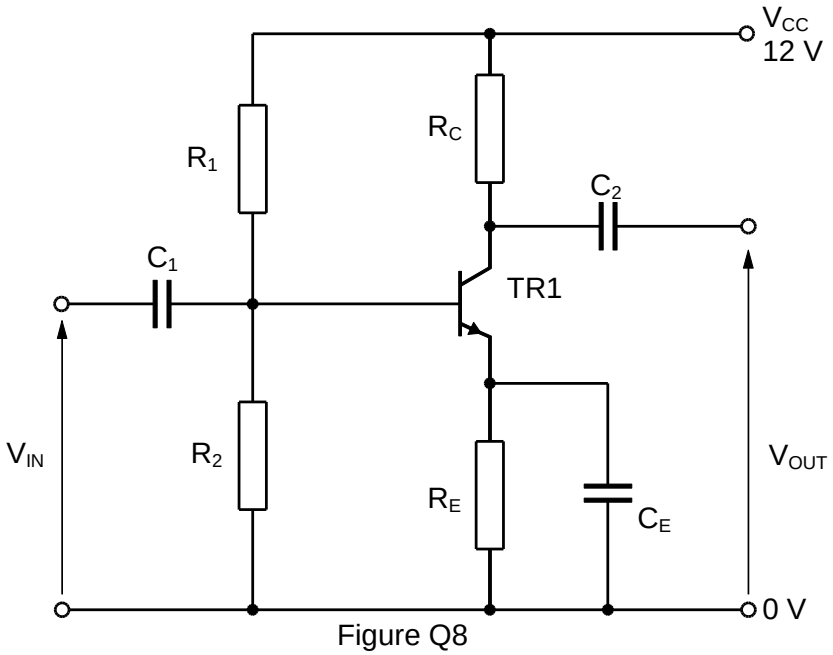


Figure Q8

(a) State the phase angle between V_{IN} and V_{OUT}.

(b) When component C_E is removed, the gain of the circuit falls drastically. Explain why the gain of the amplifier falls when C_E is removed.

(c) State the purpose of R_1 and R_2 in Figure Q8.

Answers

(a) 180° **1**

(b) The Capacitor C_E provides a bypass, around R_E for the small ac input signal, thereby allowing the input signal to have a significant effect on the base current through the transistor, allowing amplification to take place. If the capacitor is removed the bypass path is removed and the small ac input signal is restricted by R_E as this now has less effect on the base current less amplification now takes place. **3**

(c) R_1 and R_2 are the bias resistors that control the operating point of the transistor. **1**

(5)

9.

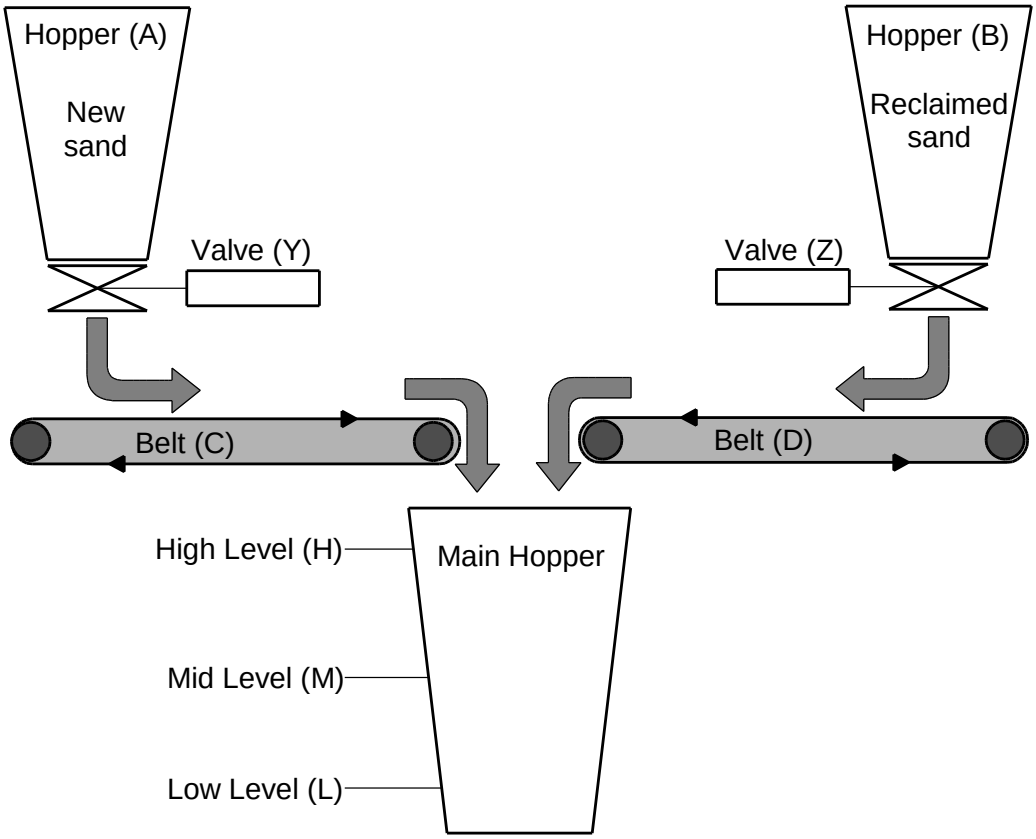


Figure Q9

The sketch in Figure Q9 shows an industrial sand mixing system. The valve (Z) on the reclaimed sand hopper (B) can only be opened if the belt (C) is stopped and the belt (D) is running and the main sand hopper is at Mid Level (M) but not at High Level (H).

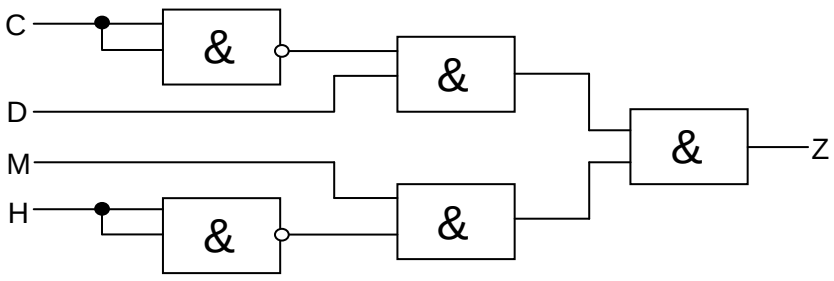
(a) Determine the logic output required to open the valve (Z).

(b) Draw, using BS symbols, a logic diagram for this system using only 2-input gates.

Answers

(a) $Z = \overline{C} \cdot D \cdot M \cdot \overline{H}$ **3**

(b)



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(6)

Section B

Attempt any TWO questions in this section (50 marks)
Each question is worth 25 marks

10. *(a)* Figure Q10*(a)* shows the currents in a circuit. Determine the currents I_1, I_2, I_3, I_4, I_5 and I_6.

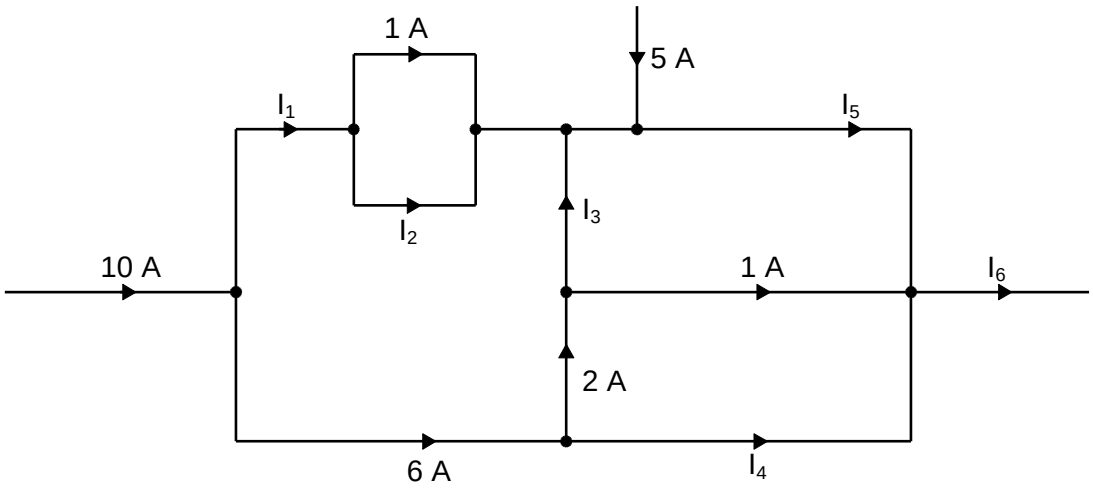


Figure Q10*(a)*

(b) Figure Q10*(b)* shows the voltages in a circuit. Determine the voltages V_1, V_2 and V_{IN}.

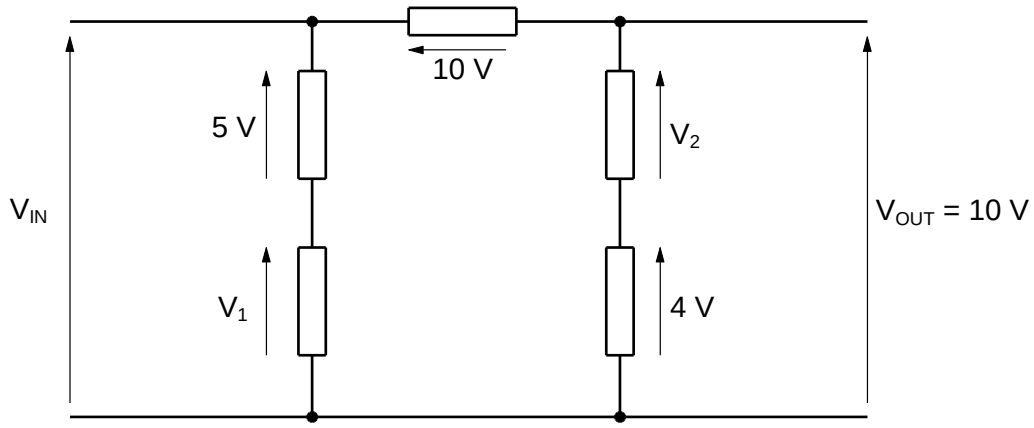


Figure Q10*(b)*

Marks

10. *(c)* For the circuit shown in Figure Q10*(c)* below, the variable resistor (R_V) can be varied between 15 Ω and 25 Ω.

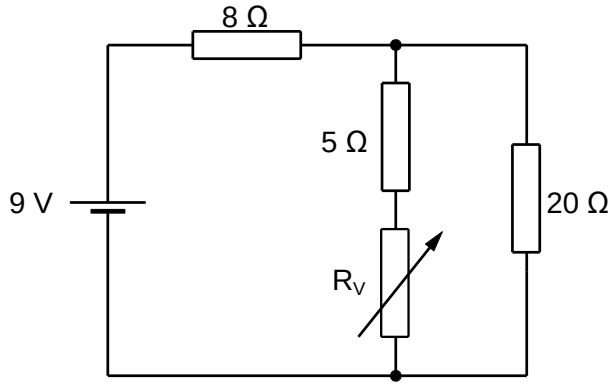


Figure Q10*(c)*

Determine:

(i) the maximum circuit resistance;
(ii) the minimum circuit resistance;
(iii) the maximum supply current;
(iv) the minimum supply current;
(v) the maximum circuit power;
(vii) the maximum power dissipated by the 8 Ω resistor;
(viii) the maximum energy consumed by the 8 Ω resistor in 1·5 hours.

Answers

(a)
$I_1 = 4$ A **1**
$I_2 = 3$ A **1**
$I_3 = 1$ A **1**
$I_4 = 4$ A **1**
$I_5 = 10$ A **1**
$I_6 = 15$ A **1**

(b)
$V_2 = 6$ V **1**
$V_1 = 15$ V **1**
$V_{IN} = 20$ V **1**

(c)

(i) $R_{MAX} = 8 + 30//20 = 20\ \Omega$ **3**

(ii) $R_{MIN} = 8 + 20//20 = 18\ \Omega$ **3**

(iii) $I_{MAX} = \dfrac{V_S}{R_{MIN}} = \dfrac{9}{18} = 0 \cdot 5\,A$ **2**

(iv) $I_{MIN} = \dfrac{V_S}{R_{MAX}} = \dfrac{9}{20} = 0 \cdot 45\,A$ **2**

(v) $P_{MAX} = V_S \times I_{MAX} = 9 \times 0{\cdot}5 = 4{\cdot}5$ W **2**

(vi) $P_{MAX\,8\Omega} = I_{8\Omega}^2 \times R = 0{\cdot}5^2 \times 8 = 2$ W **2**

(viii) $E_{MAX\,8\Omega} = P \times t = 1{\cdot}5 \times 60 \times 90 = 8{\cdot}1$ kJ **2**

(25)

11. *(a)* Add the following binary numbers.

(i) $1100_2 + 0101_2$

(ii) $0111_2 + 1101_2$

(b) Draw the logic circuit using ANSI symbols for the following logic expression.

$$Z = \overline{A}.B + \overline{A.C} + \overline{\overline{A}.\overline{B}.\overline{C}}$$

(c) For the circuit shown in Figure Q11*(c)*,

(i) state the type of gate used;

(ii) determine the logic level at points A and C when point B is Low (logic 0).

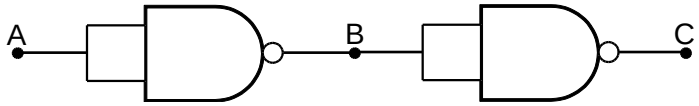


Figure Q11*(c)*

(d) For the circuit shown in Figure Q11*(d)*,

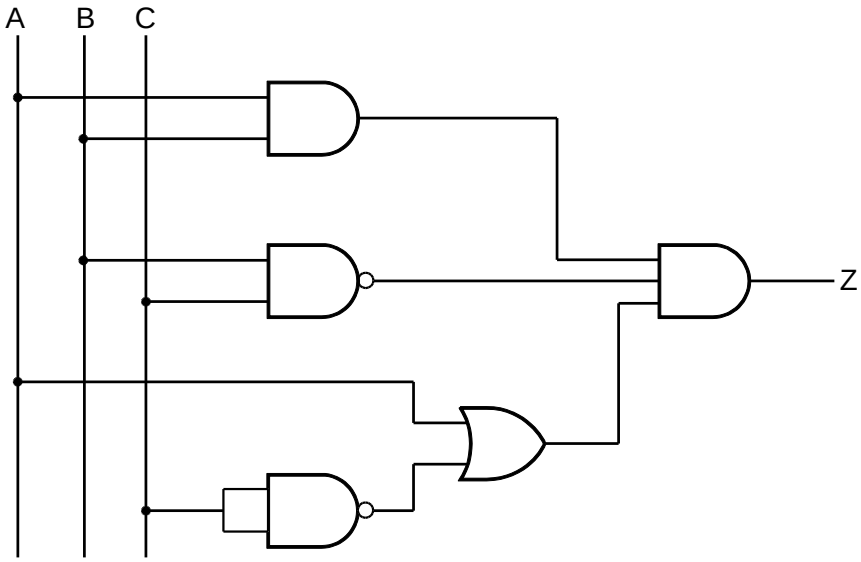


Figure Q11*(d)*

(i) determine the circuit Boolean expression;

(ii) construct the circuit truth table.

A fault condition causes all the NAND gate outputs to be High (logic 1).

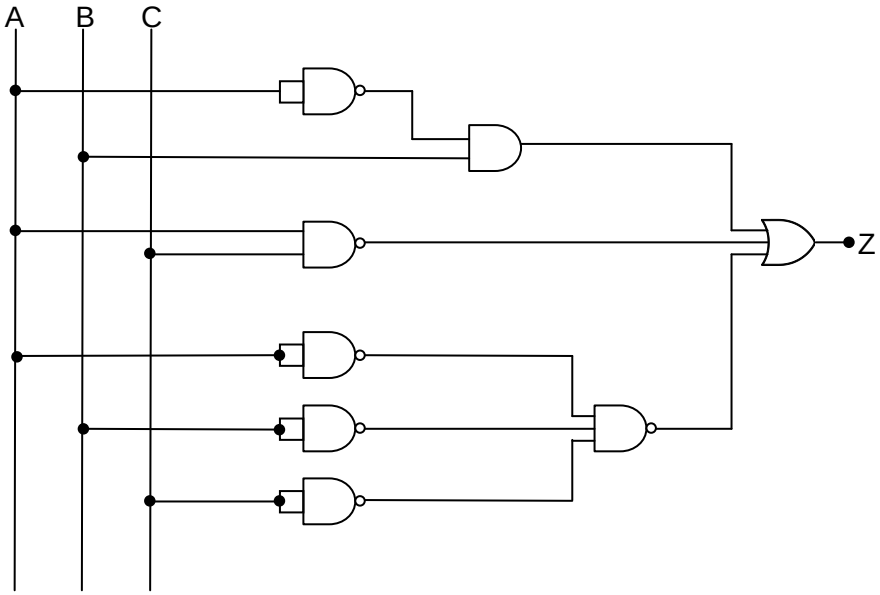
(iii) Determine the new outputs for Z.

Answers

11. *(a)* (i) 10001_2 **2**

(ii) 10100_2 **2**

(b)



NOT gates can be used instead of the tied 2-input NAND's **4**

(c) (i) 2-input NAND **1**

(ii) Point A = High (1)
Point C = High (1) **2**

(d) (i) $Z = (A.B).\overline{(B.C)}.(A + \overline{C})$ **3**

(ii) & (iii)

INPUTS			GATE OUTPUT						Fault Condition
A	B	C	A.B 1	$\overline{B.C}$ 2	A	$\overline{C}$	$A + \overline{C}$ 3	Z 1.2.3	
0	0	0	0	1	0	1	1	0	0
0	0	1	0	1	0	0	0	0	0
0	1	0	0	1	0	1	1	0	0
0	1	1	0	0	0	0	0	0	0
1	0	0	0	1	1	1	1	0	0
1	0	1	0	1	1	0	1	0	0
1	1	0	1	1	1	1	1	1	1
1	1	1	1	0	1	0	1	0	1

8
3

(25)

Marks

12. *(a)* For the circuit shown in Figure Q12*(a)* below, the variable resistor (R_V) can be varied between 5 kΩ and 15 kΩ.

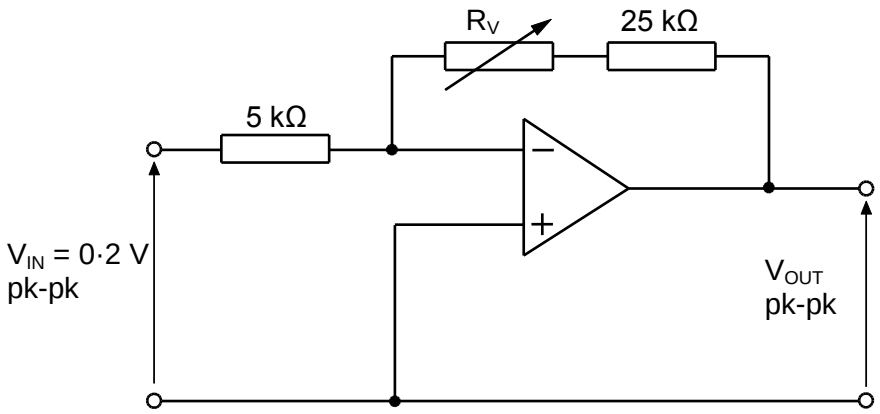


Figure Q12*(a)*

(i) Name the circuit configuration.

(ii) State the names given to the input terminals labelled '–' and '+'.

Determine:

(iii) the maximum $V_{OUT\ pk\text{-}pk}$;

(iv) the minimum $V_{OUT\ pk\text{-}pk}$;

(v) the value of R_V required to give a $V_{OUT\ pk\text{-}pk}$ of 1·4 V.

12. *(b)* For the circuit shown in Figure Q12*(b)* below,

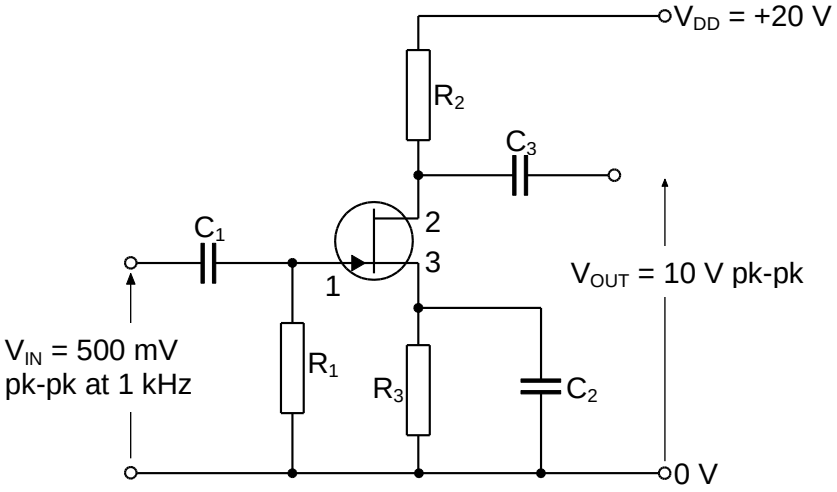


Figure Q12*(b)*

(i) name the circuit configuration;

(ii) name the transistor terminals 1, 2 and 3;

(iii) determine the circuit gain;

(iv) determine the peak (pk) output voltage;

(v) state the purpose of the capacitor C_3.

(c) The circuit shown in Figure Q12(*c*) is used to control the power supplied to a lamp.

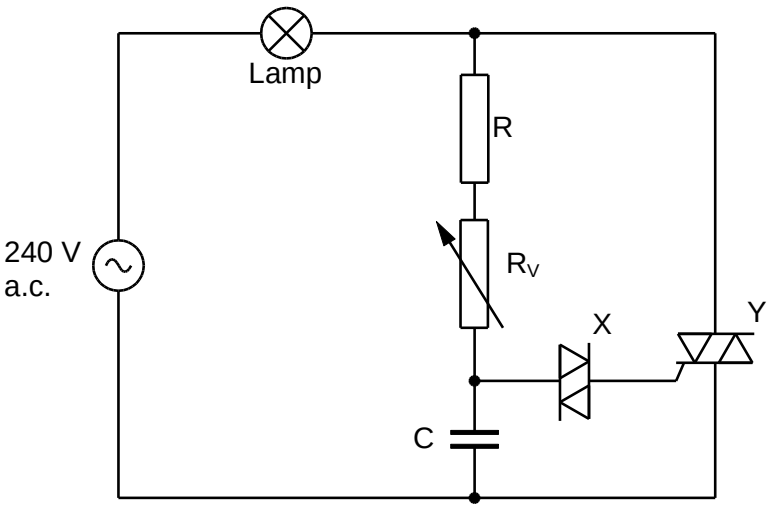


Figure Q12*(c)*

(i) Name the components labelled X and Y.

(ii) Explain the purpose of R_V.

Marks

Answers

12. *(a)* (i) Inverting amplifier **1**

(ii) Inverting and Non-inverting inputs **2**

(iii) $V_{OUT\ max} = 1{\cdot}6$ V **2**

(iv) $V_{OUT\ min} = 1{\cdot}2$ V **2**

(v) R_V = 10 kΩ **3**

(b) (i) FET amplifier **2**

(ii) 1 – Gate
2 – Drain
3 – Source **3**

(iii) Gain = $\frac{10}{0{\cdot}5} = 20$ **2**

(iv) V_{pk} = 5 V **1**

(v) C3 is a coupling capacitor and it is used to block (remove) the d.c. component. **2**

(c) (i) X = Diac and Y = Triac **2**

(ii) R_V controls the rate at which the capacitor charges and therefore the time can be varied as to when the diac gate current triggers the triac. **3**

(25)

[END OF MARKING INSTRUCTIONS]