2011 Electronic and Electrical Fundamentals

Intermediate 2

Finalised Marking Instructions

Marks

Section A

Attempt all the questions in this section (50 marks)

1. Convert the following numbers.

(a) Binary to decimal 10101111_2

(b) Decimal to Hexadecimal 123_{10}

(c) Hexadecimal to Binary CD_{16}

Answers

(a)	10101111_2	=	175_{10}	**2**
(b)	123_{10}	=	$7B_{16}$	**2**
(c)	CD_{16}	=	11001101_2	**2**
				(6)

2. Identify the pin connections for the circuit symbols shown in Figure Q2*(a)* and Figure Q2*(b)*.

(a)

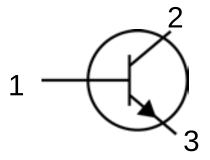


Figure Q2*(a)*

(b)

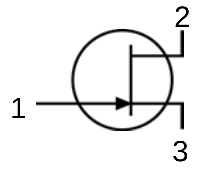


Figure Q2*(b)*

Answers

(a) 1 = base, 2 = collector, 3 = emitter **3**

(b) 1 = gate, 2 = drain, 3 = source **3**

(6)

3. *(a)* For the circuit shown in Figure Q3*(a)* below, determine:

(i) the voltage V_{AE};

(ii) the voltage V_{AB};

(iii) the voltage V_{CD};

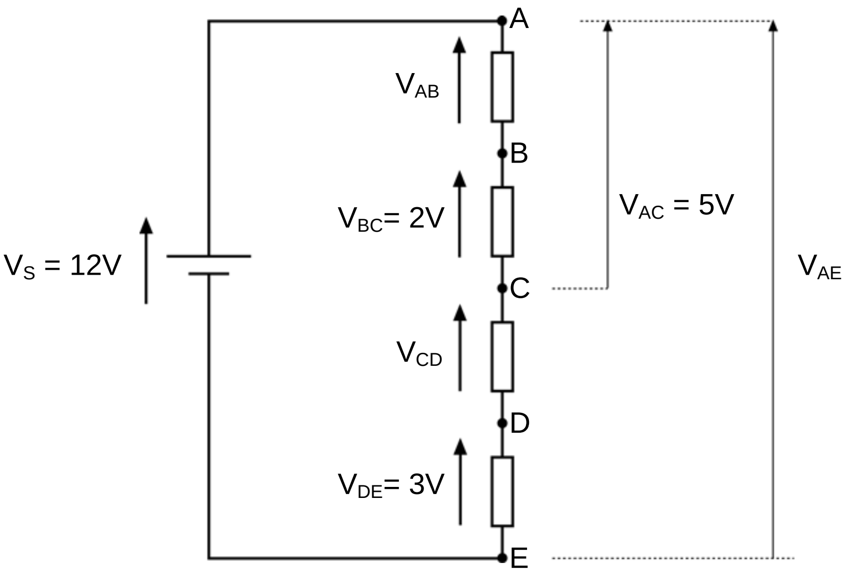


Figure Q3*(a)*

(b) For the circuit shown in Figure Q3*(b)* below, determine:

(i) I_1;

(ii) I_2;

(iii) I_3;

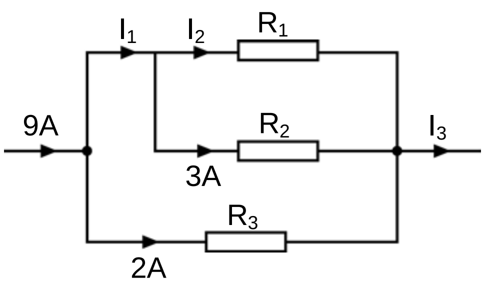


Figure Q3*(b)*

Answers

(a)	(i)	$V_{AE} = 12V$	**1**
	(ii)	$V_{AB} = 3V$	**1**
	(iii)	$V_{CD} = 4V$	**1**
(b)	(i)	$I_1 = 7A$	**1**
	(ii)	$I_2 = 4A$	**1**
	(iii)	$I_3 = 9A$	**1**
			(6)

4. Determine the logic input X, Y and Z for each of the guests in Figure Q4*(a)*, Figure Q4*(b)* and Figure Q4*(c)*.

(*a*)

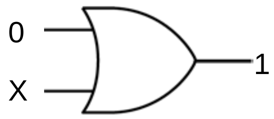


Figure Q4*(a)*.

(*b*)

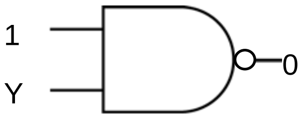


Figure Q4*(b)*.

(c)

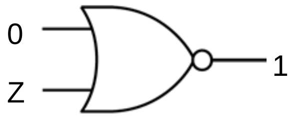


Figure Q4*(c)*.

Answers

(a)	X = 1	**1**
(b)	Y = 1	**1**
(c)	Z = 0	**1**
		(3)

5. For the circuit shown in Figure Q5:

(a) name the circuit configuration;

(b) determine the circuit gain.

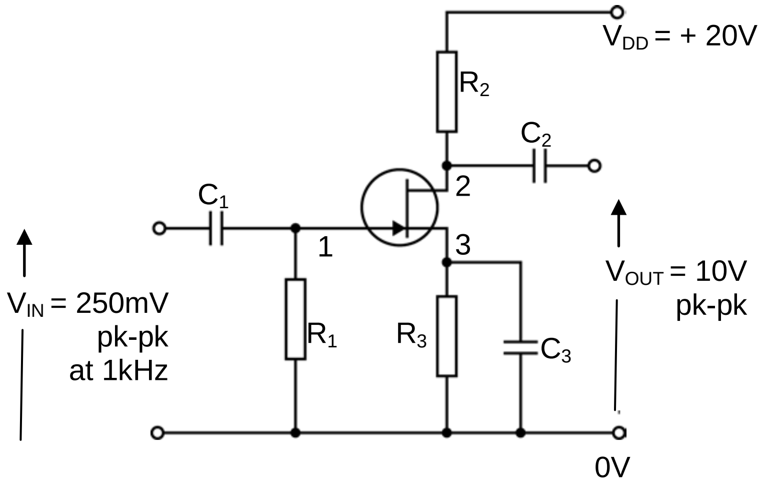


Figure Q5

Answers

(a) Common Source Amplifier or FET Amplifier. **1**

(b) Gain = V_{out}/Vin = 10/0.25 = 40 or -40 **2**

(3)

Marks

6. Figure Q6 shows a current carrying conductor placed between the poles of a magnet.

Figure Q6

State the effect on the force acting upon the conductor when:

(a) the current is doubled;

(b) the current direction is reversed;

(c) the poles are reversed;

(d) a stronger magnet is used.

Answers

(a)	Force doubles or increases	**1**
(b)	Force changes direction or reversed	**1**
(c)	Force changes direction or reversed	**1**
(d)	Force is stronger	**1**
		(4)

7. The diagram in Figure Q7 includes a variable resistor (R_V) that can be varied between 1 kΩ and 10 kΩ.

(a) Determine the output voltage (pk-pk) when R_V is 8 kΩ.

(b) Determine the minimum value of output voltage (pk-pk).

(c) Explain why an output voltage of 500 mV (pk-pk) is not achievable with the 50 mV (pk-pk) input voltage.

(d) Determine the new value of input voltage that would enable an output voltage of 500 mV (pk-pk) to be achieved when R_V is set for maximum gain.

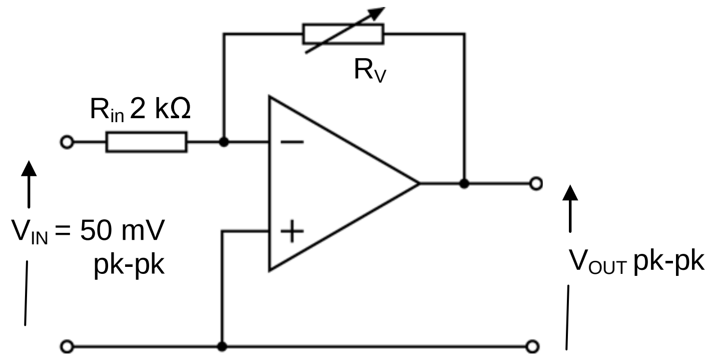


Figure Q7

Answers

(a)	V_{out} = 4 x 50m = 200m V pk-pk	**2**
(b)	$V_{out\ min}$ = ½ x 50m V = 25m V pk-pk	**2**
(c)	A V_{out} OF 500M v requires a gain of 10 but the maximum possible is only 5	**2**
(d)	$V_{IN} = V_{OUT}$/Gain = 500m V/5 = 100m V pk-pk	**2** **(8)**

8. For the circuit shown in figure Q8.

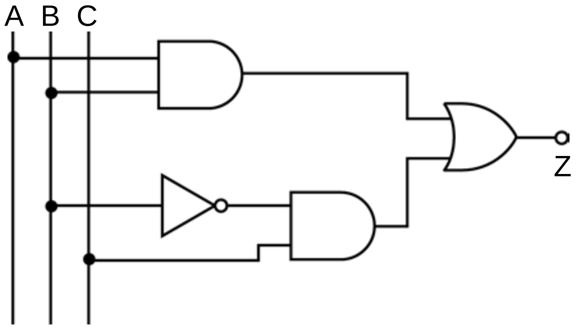


Figure Q8

(a) determine the Boolean expression for output Z;

(b) draw the truth table for the circuit.

(c) A fault condition causes the invertor output to be permanently High.
Complete the truth table for this condition.

Answers

(a) $Z = A.B + \overline{B}.C$ **2**

(b)&(c) **4 & 2**

			1	2	1 + 2	Fault
A	B	C	A.B	$\overline{B}.C$	Z	Z
0	0	0	0	1	0	0
0	0	1	0	0	1	1
0	1	0	0	1	0	0
0	1	1	0	1	0	1
1	0	0	0	1	0	0
1	0	1	0	0	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

(8)

9. For the circuit shown in Figure Q9, state:

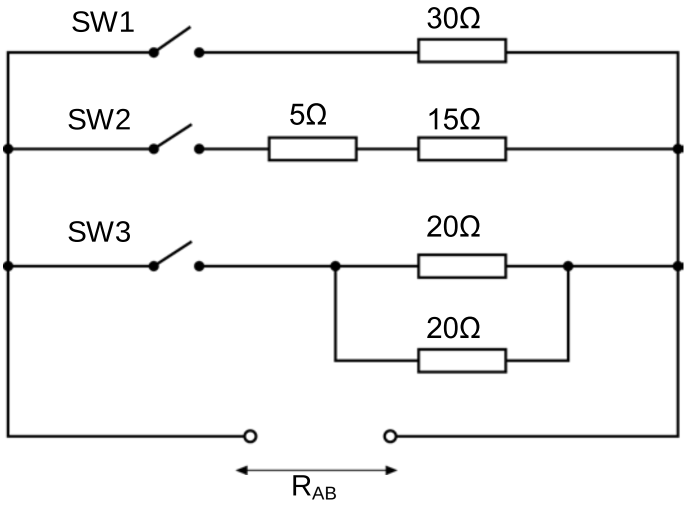


Figure Q9

(a) which switch(es) should be closed to give minimum R_{AB};

(b) which switch(es) should be closed to give maximum R_{AB};

(c) which switch(es) should be closed to make R_{AB} 12Ω.

Answers

(a) All SW's should be closed **2**

(b) SW1 **2**

(c) SW1 & SW2 **2**

(6)

Section B

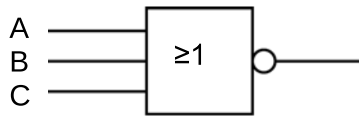
Attempt any TWO questions in this section (50 marks)
Each question is worth 25 marks

10. Add the following binary numbers.

(a) (i) $0011_2 + 0111_2$

(ii) $0100_2 + 0111_2$

(b) State the Boolean expression and construct the truth table for the following logic gate.



(c) Using the datasheet provided, select the required logic chip and mark the logic chip number and pin numbers on the logic diagram on Worksheet Q10*(c)*.

Note: You may use any of the 6 logic chips and each logic chip may only be used once.

(d) Draw, using BS symbols, the logic diagram for the following Boolean expression and determine the truth table.

$Z = (\overline{R} + S + \overline{T}).(S + T)$

(e) The circuit shown below Figure 10*(e)*(i) has developed a fault and upon testing the outputs shown in the truth table Figure 10*(e)*(ii) were obtained. Determine which gate (input or output) is at fault and state the nature of the fault.

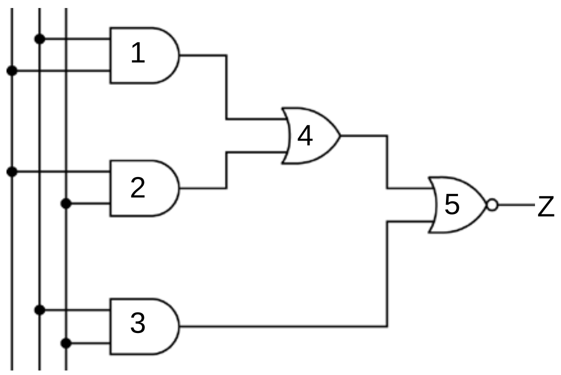


Figure 10*(e)*(i)

A	B	C	Z
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Figure 10*(e)*(ii)

Answers

(a) (i) $0011_2 + 0111_2 = 1010_2$ **2**

(ii) $0100_2 + 0111_2 = 1011_2$ **2**

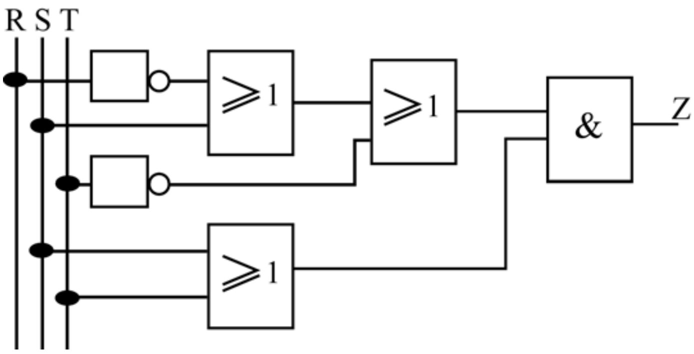
(b) $Z = \overline{A + B + C}$ **1**

2

A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

(c) See Worksheet **6**

(d) $Z = (\bar{R} + S + \bar{T}).(S + T)$ **2**



4

R	S	T	$\bar{R} + S + \bar{T}$	S + T	**Z**
0	0	0	1	0	**0**
0	0	1	1	1	**1**
0	1	0	1	1	**1**
0	1	1	1	1	**1**
1	0	0	1	0	**0**
1	0	1	0	1	**0**
1	1	0	1	1	**1**
1	1	1	1	1	**1**

(e) 4

			1	2	1+2	INV	
A	B	C	(A,B)+A.C	B.C		Z	**FAULT**
0	0	0	0	0	0	1	**1**
0	0	1	0	0	0	1	**1**
0	1	0	0	0	0	1	**1**
0	1	1	0	1	1	0	**1**
1	0	0	0	0	0	1	**1**
1	0	1	1	0	1	0	**0**
1	1	0	1	0	1	0	**0**
1	1	1	1	1	1	0	**0**

Marks awarded for construction/derivation of truth table and identifying the location of the faulty output.

Fault occurs when input B and C are on and the output of gate 3 and/or the input of gate 5 is held low. 2

11. *(a)* For the wave form to be shown in Figure Q11*(a)* determine:

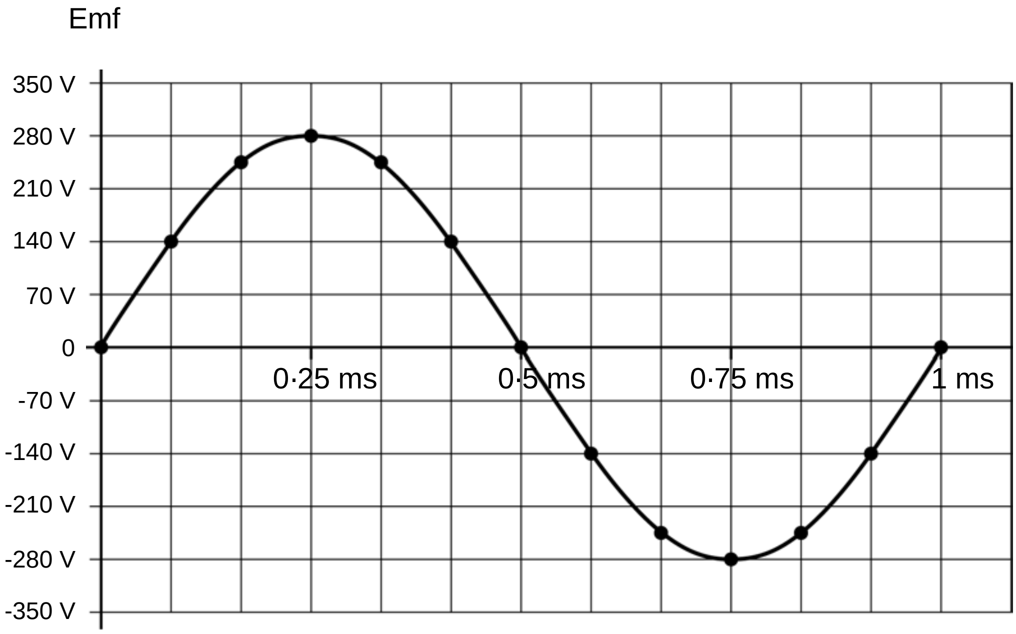


Figure Q11*(a)*

(i) the peak value of the voltage;

(ii) the rms value;

(iii) the period of the waveform.

(b) (i) A coil of length 0·5m is moved through a magnet field of 0·25 T at a speed of 10 ms^{-1}. Calculate the induced voltage.

(ii) The same coil is now inserted in a management field of 1·2 T and is connected to a supply. Determine the current flowing in the conductor if the force on the conductor is measured at 2·4 N.

(c) For the circuit shown in Figure Q11*(c)* determine:

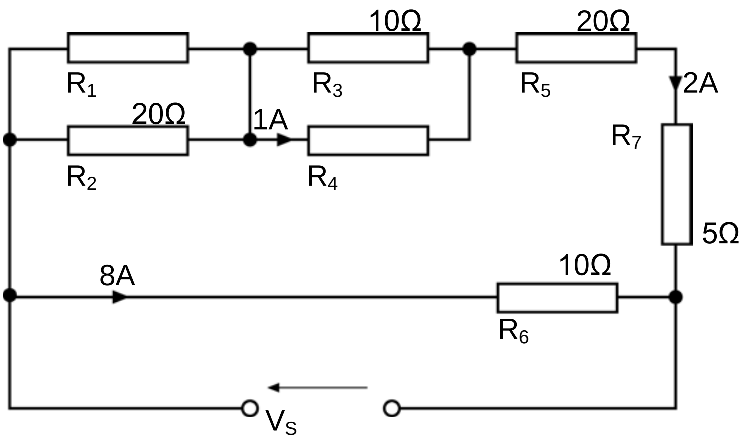


Figure Q11*(c)*

(i) the supply voltage V_s;

(ii) the total circuit resistance;

(iii) the current through resistor R_3;

(iv) the voltage across resistor R_3;

(v) the value of resistor R_4;

(vi) the voltage across resistor R_1;

(vii) The value of resistor R_1.

(d) For the circuit shown in Figure Q11*(d)* determine:

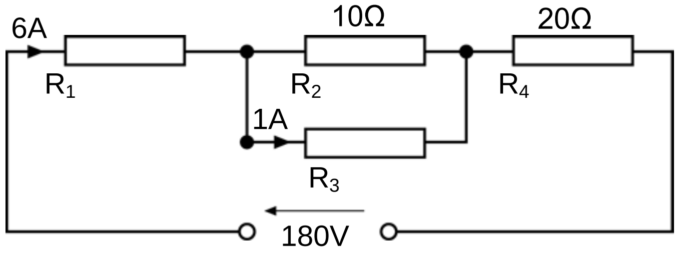


Figure Q11*(d)*

(i) the power dissipated in the 10Ω resistor R_2;

(ii) the total power dissipated in the circuit;

(iii) the energy consumed, in Joules, if the circuit is operated for 2 hours.

Answers

(a)	(i)	The peak value is **280V**	**1**
	(ii)	The rms = 280 x 0.707 = **197·96V**	**2**
	(iii)	Period = **1ms**	**1**
(b)	(i)	E = B x l x v = 0.25 x 0.5 x 10 = **1.25V**	**2**
	(ii)	F = B x I x l hence I = F/(B x 1)	**3**
		I = 2.4/(1.2 x .5) = **4A**	
(c)	(i)	$V_S = I_{R6} \times R_6$ = 8 x 10 = **80V**	**2**
	(ii)	$I_T = I_{R6} + I_{R5}$ = 8 + 2 = 10A	**2**
		$R_T = V_S/I_T$ = 80/10 = 8Ω	
	(iii)	Current in R_3 (by Kirchhoff's) = 2 – 1 = **1A**	**1**
	(iv)	$V_{R3} = I_{R3} \times R_3$ = 1 x 10 = **10V**	**1**
	(v)	R4 = V_{R3}/I_{R4} = 10/1 = **10Ω** or	**1**
		As $I_{R3} = I_{R4}$ and $V_{R3} = V_{R4}$ then $R_3 = R_4$	
	(vi)	V_{R3} = 10V; V_{R5} = 2 x 20 = 40V; V_{R7} = 2 x 5 = 10V;	**2**
		Therefore by Kirchhoff's	
		$V_{R1} = V_s – V_{R3} - V_{R5} – V_{R7}$ = 80 – 1- - 40 – 10 = **20V**	
	(vii)	R_1, R_2 combination = $V_{R1}/I_{R1} + I_{R2}$ = 20/2 = 10Ω	**2**
		Therefore as R_2 = 20Ω then R_1 must = **20Ω**	
		Or	
		$I_{R2} = V_{R1}/R_2$ = 20/20 = 1A therefore by Kirchhoff's	
		$I_{R1} = I_{R7} – I_{R2}$ = 2 – 1 = 1A hence R1 = V_{R1}/I_{R1} = 20/1 = **20Ω**	
(d)	(i)	I_{R2} = 6 – 1 = 5A	**2**
		$P = I^2 \times R$ = 5 x 5 x 10 = **250W**	
	(ii)	PT = $V_S \times I_S$ = 180 x 6 = **1080W**	**1**
	(iii)	E = P x t = 1080 x 2 x 60 x 60 = **7776000J = 7.776MJ**	**2**

Marks

12. *(a)* Identify the circuit shown in Figure Q12*(a)* and identify the purpose of each of the capacitators C_1, C_2, and C_3. **4**

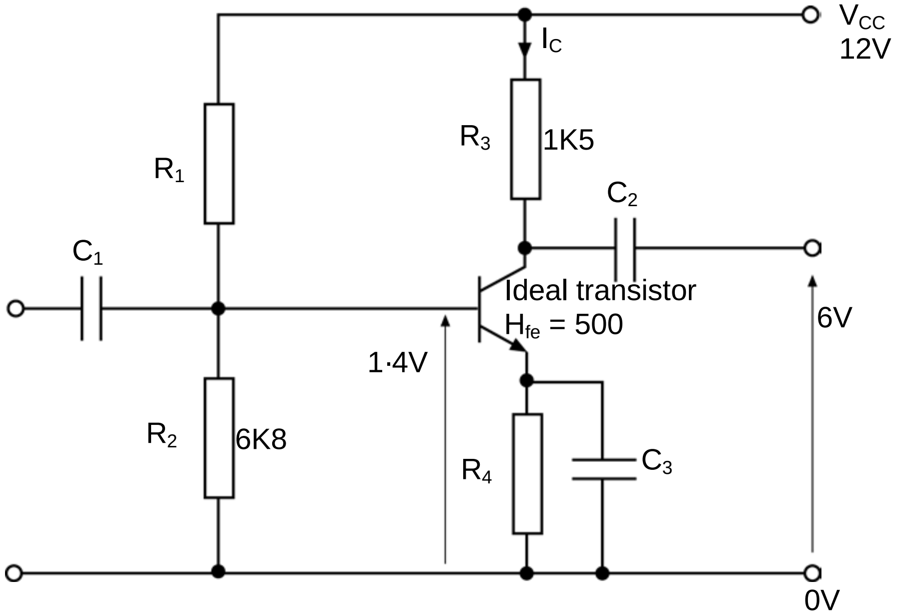


Figure Q12*(a)*

(b) For the circuit shown in Figure Q12*(a)* calculate:

(i) the collector current I_C;

(ii) the base current I_b;

(iii) the current through the resistor R_2;

(iv) the value of the resistor R_1.

(c) For the circuit shown in Figure Q12*(c)*.

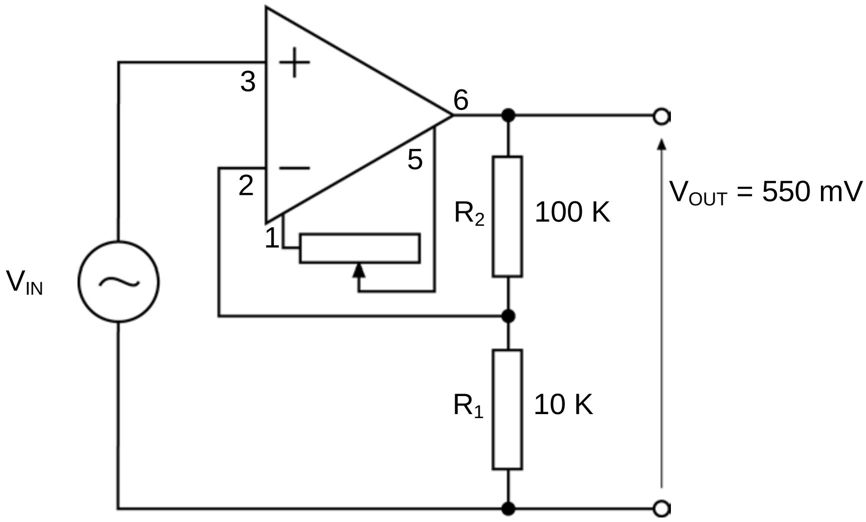


Figure Q12*(c)*

(i) Identify the circuit configuration shown in Figure Q12*(c).*

(ii) Determine the gain of the circuit and the input voltage.

(iii) When setting up the circuit it is found that for an input of 0 V the output is not zero. What component in Figure Q12*(c)* will allow the output to be adjusted to zero? What is this process called?

(d)

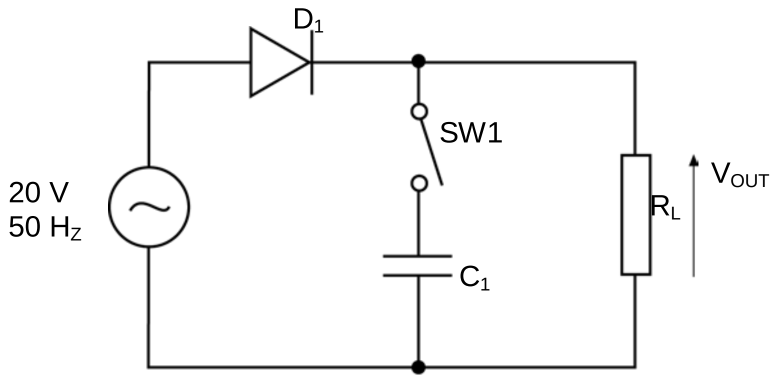


Figure Q12*(d)*

Sketch the output waveform for the circuit in Figure Q12*(d)* with

(A) SW1 open, and

(B) SW1 closed.

Answers

12. *(a)* Common Emitter Amplifier **1**
C1: - Coupling Capacitor **1**
C2: - Coupling Capacitor **1**
C3: - Decoupling Capacitor or Bypass Capacitor **1**

(b) (i) By Kirchhoff's $V_{R3} = V_S - V_{OUT} = 12 - 6 = 6V$ **2**

$I_{R3} = V_{R3}/R_3 = 6/1500 =$ **4mA**

(ii) Gain = 500 = Ic/Ib hence Ib = I c/Gain = 4mA/500 = **8µA** **2**

(iii) $I_{R2} = V_{R2}/R_2 = 1.4/6800 =$ **206µA** **2**

(iv) $I_{R1} = + Ib = 206 + 8 = 214µA$ **2**

$I_{R1} = V_S - V_{R2} = 12 - 1.4 - 10.6V$

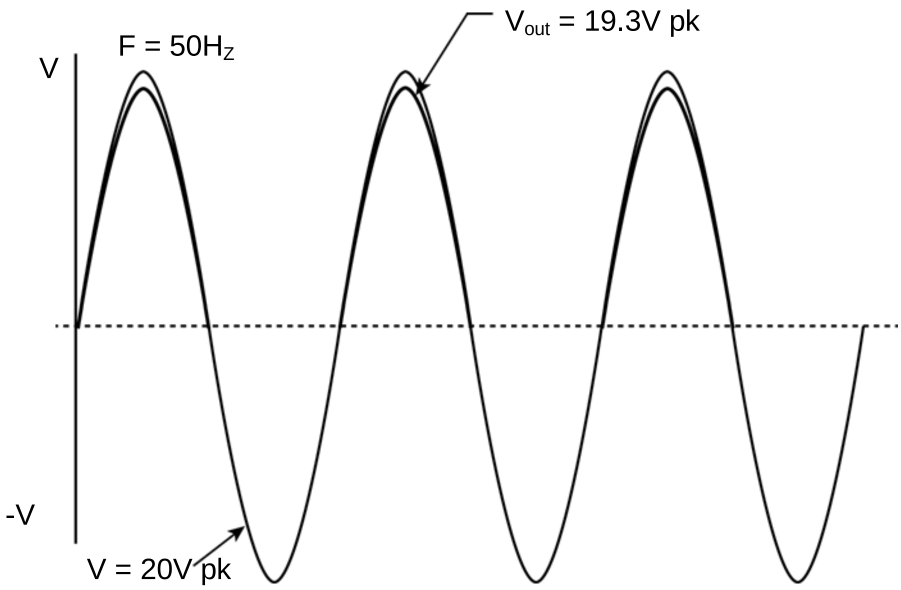
Hence $R_1 = C/I_{R1} = 10.6/214µA =$ **49.53kΩ**

(c) (i) Non inverting Op Amp **1**

(ii) Gain = $(R_2/R_1) + 1 = (100/10) + 1 = 10 + 1 = 11$ **2**

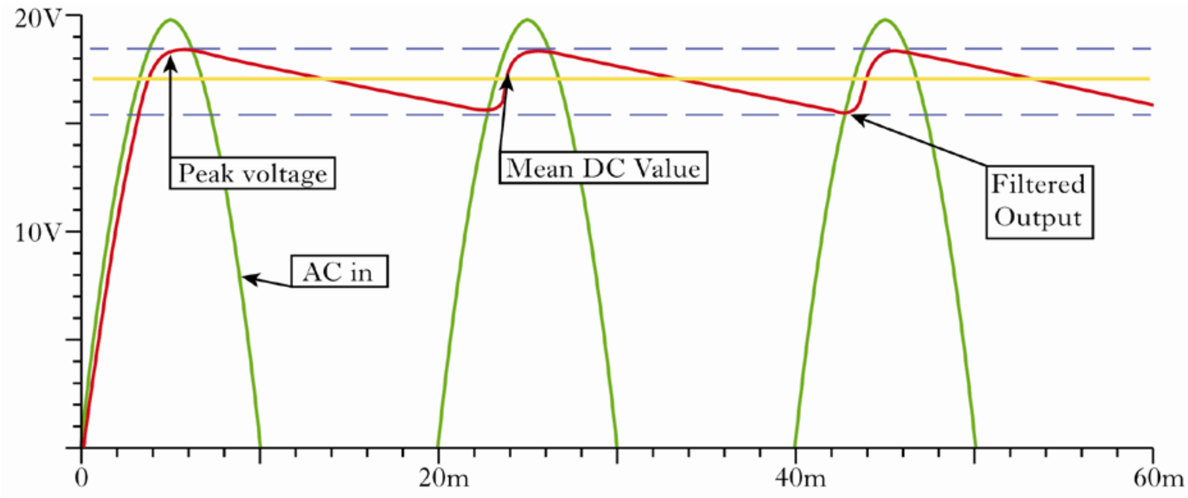
(iii) **Gain = V_{out}/Vin** **2**
Hence Vin = V_{out}/gain = 550m V/11 = 50m V

(d)



(A) By adjusting the variable resistor Rv **1**

(B) Offset Null adjustment **2**



[END OF MARKING INSTRUCTIONS]