X025/201

NATIONAL QUALIFICATIONS 2011

TUESDAY, 7 JUNE 1.00 PM – 3.30 PM

ELECTRONIC AND ELECTRICAL FUNDAMENTALS
INTERMEDIATE 2

100 marks are allocated to this paper.

Answer **all** questions in Section A (50 marks).

Answer **two** questions from Section B (25 marks each).

A Datasheet is provided for question 10(*c*).

A Worksheet is provided for question 10(*c*).

In all your answers to questions requiring calculations, all working **must** be shown.

Marks

Section A

Attempt all the questions in this section (50 marks)

1. Convert the following numbers.

(*a*) Binary to decimal 10101111_2 **2**

(*b*) Decimal to hexadecimal 123_{10} **2**

(*c*) Hexadecimal to Binary CD_{16} **2**

(6)

2. Identify the pin connections for the circuit symbols shown in Figure Q2(*a*) and Figure Q2(*b*).

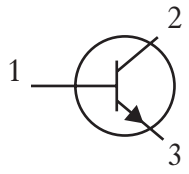


Figure Q2(*a*) **3**

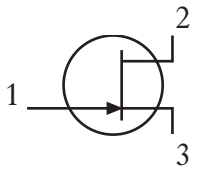


Figure Q2(*b*) **3**

(6)

Marks

3. (*a*) For the circuit shown in Figure Q3(*a*) below, determine:

(i) the voltage V_{AE}; **1**

(ii) the voltage V_{AB}; **1**

(iii) the voltage V_{CD}. **1**

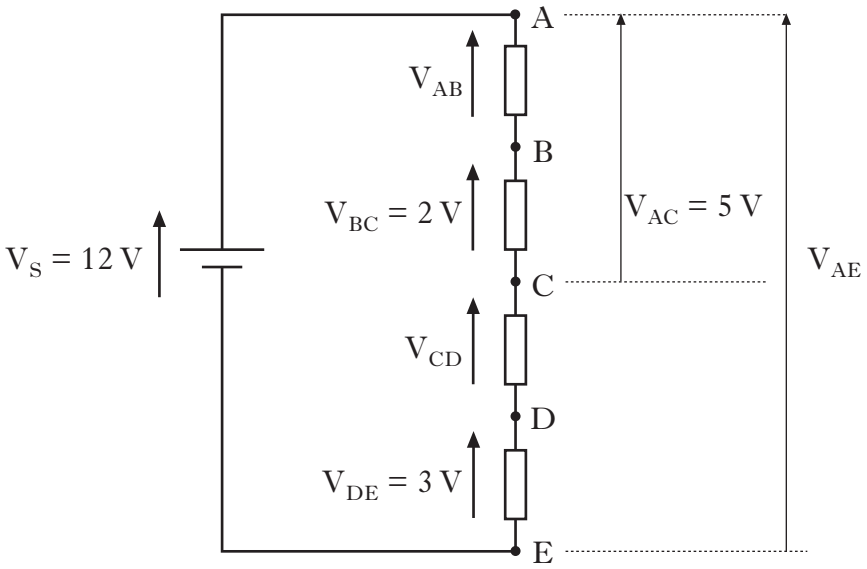


Figure Q3(*a*)

(*b*) For the circuit shown in Figure Q3(*b*) below, determine:

(i) I_1; **1**

(ii) I_2; **1**

(iii) I_3. **1**

(6)

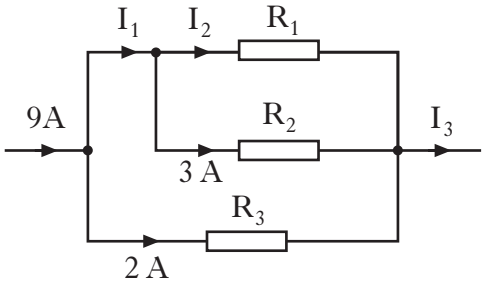


Figure Q3(*b*)

[Turn over

Marks

4. Determine the logic input X,Y and Z for each of the gates shown in Figure Q4(*a*), Figure Q4(*b*) and Figure Q4(*c*).

(*a*)

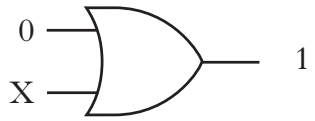


Figure Q4(*a*) **1**

(*b*)

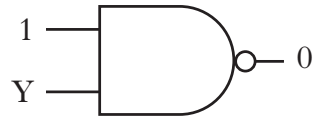


Figure Q4(*b*) **1**

(*c*)

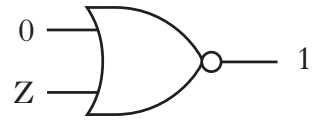


Figure Q4(*c*) **1**

(3)

Marks

5. For the circuit shown in Figure Q5:

(*a*) name the circuit configuration; **1**

(*b*) determine the circuit voltage gain. **2**

(3)

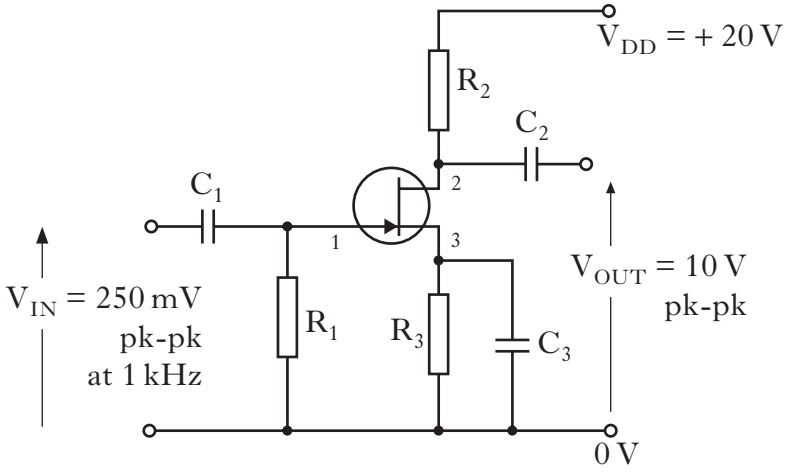


Figure Q5

6. Figure Q6 shows a current carrying conductor placed between the poles of a magnet.

Figure Q6

State the effect on the force acting upon the conductor when:

(*a*) the current is doubled; **1**

(*b*) the current direction is reversed; **1**

(*c*) the poles are reversed; **1**

(*d*) a stronger magnet is used. **1**

(4)

[Turn over

Marks

7. The diagram in Figure Q7 includes a variable resistor (R_V) that can be varied between 1 kΩ and 10 kΩ.

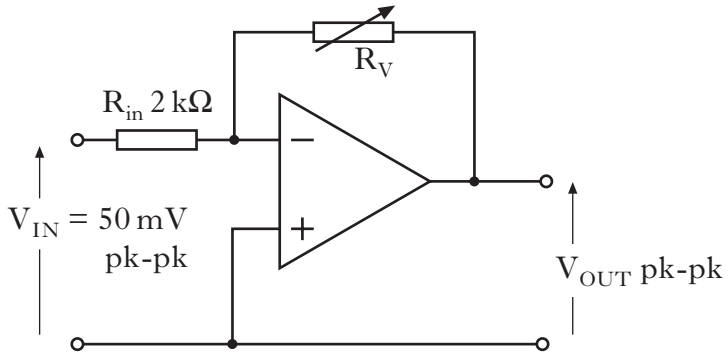


Figure Q7

(*a*) Determine the output voltage (pk-pk) when R_V is 8 kΩ. **2**

(*b*) Determine the minimum value of output voltage (pk-pk). **2**

(*c*) Explain why an output voltage of 500 mV (pk-pk) is not achievable with the 50 mV (pk-pk) input voltage. **2**

(*d*) Determine the new value of input voltage that would enable an output voltage of 500 mV (pk-pk) to be achieved when R_V is set for maximum gain. **2**

(8)

8. For the circuit shown in Figure Q8:

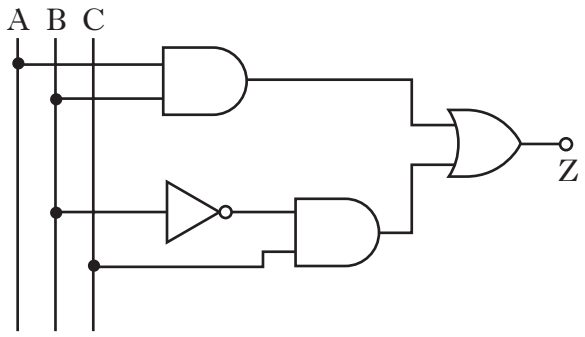


Figure Q8

(*a*) determine the Boolean expression for output Z; **2**

(*b*) draw the truth table for the circuit. **4**

(*c*) A fault condition causes the invertor output to be permanently High.
Complete the truth table for this condition. **2**

(8)

Marks

9. For the circuit shown in Figure Q9, state:

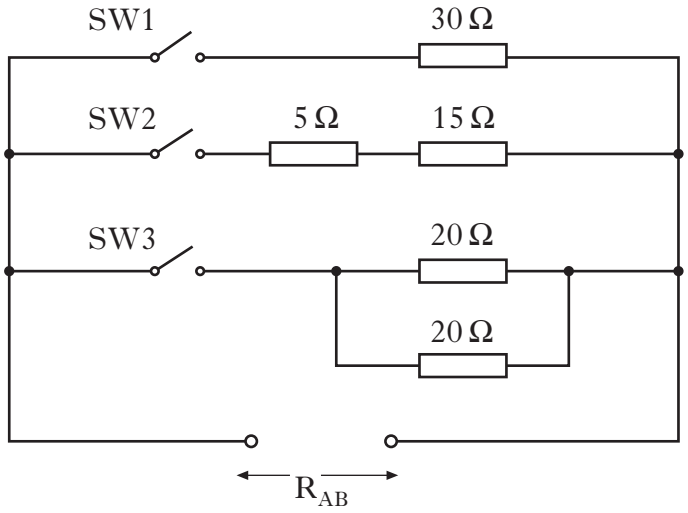


Figure Q9

(*a*) which switch(es) should be closed to give minimum R_{AB}; **2**

(*b*) which switch(es) should be closed to give maximum R_{AB}; **2**

(*c*) which switch(es) should be closed to make R_{AB} 12 Ω. **2**

(6)

Total Marks (50)

[Turn over

Marks

Section B

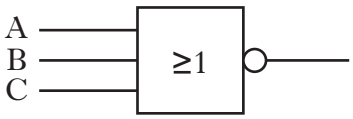
Attempt any TWO questions in this section (50 marks)
Each question is worth 25 marks

10. (*a*) Add the following binary numbers.

(i) $0011_2 + 0111_2$ **2**

(ii) $0100_2 + 0111_2$ **2**

(*b*) (i) State the Boolean expression for the following logic gate. **1**



(ii) Construct the truth table for this logic gate. **2**

(*c*) Using the Datasheet provided, select the required logic chips and mark the logic chip number and pin numbers on the logic diagram on Worksheet Q10(*c*). **6**

Note: You may use any of the 6 logic chips and each logic chip may only be used once.

(*d*) (i) Draw, using BS symbols, the logic diagram for the following Boolean expression. **2**

$Z = (\overline{R}+S+\overline{T}) \cdot (S+T)$

(ii) Construct the truth table for this expression. **4**

(*e*) The circuit shown below in Figure 10(*e*)(i) has developed a fault and upon testing the outputs shown in the truth table Figure 10(*e*)(ii) were obtained. Determine which gate (input or output) is at fault and state the nature of the fault. **6**

(25)

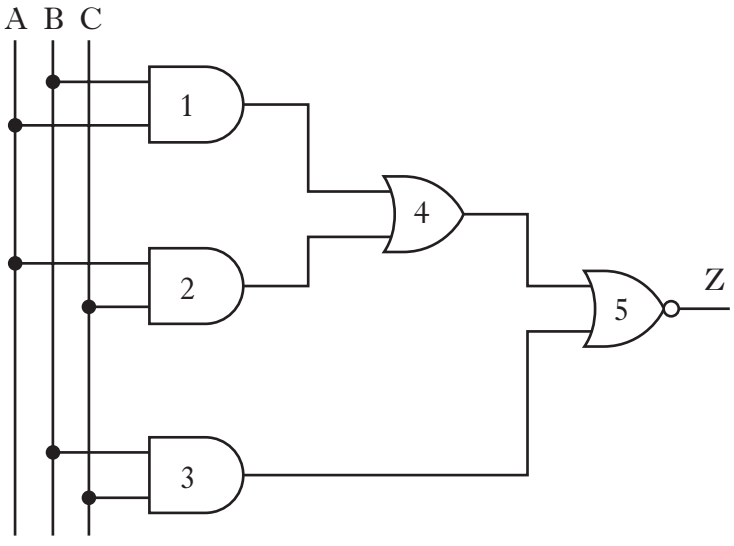


Figure 10(*e*)(i)

A	*B*	*C*	*Z*
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Figure 10(*e*)(ii)

Marks

11.

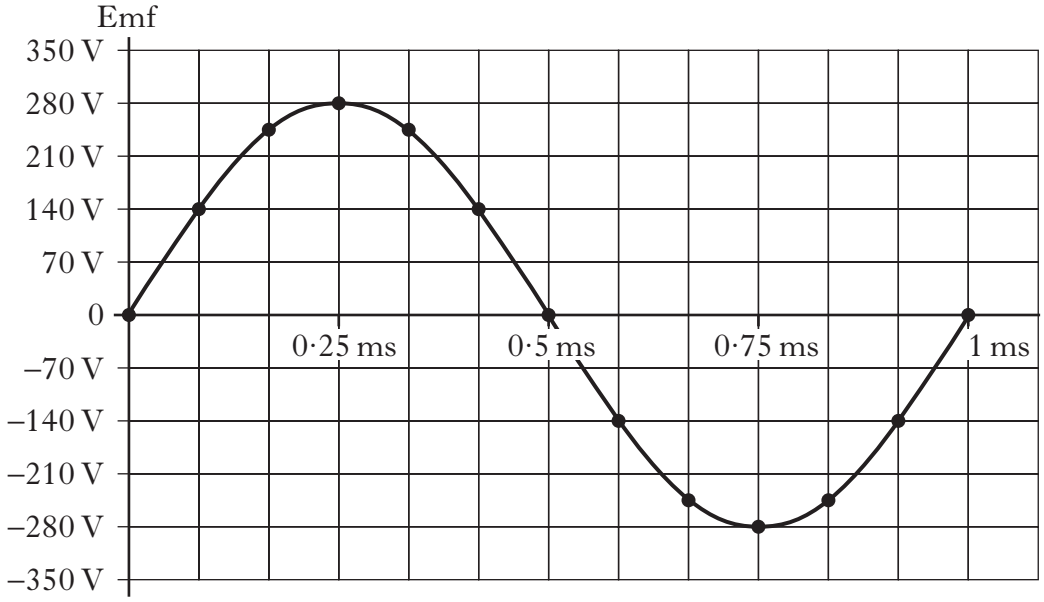


Figure Q11(*a*)

(*a*) For the waveform shown in Figure Q11(*a*) determine:

(i) the peak value of the voltage; **1**

(ii) the rms value; **2**

(iii) the period of the waveform. **1**

(*b*) (i) A coil of length 0·5 m is moved through a magnet field of 0·25 T at a speed of 10 ms^{-1}. Calculate the induced voltage. **2**

(ii) The same coil is now inserted in a magnet field of 1·2 T and is connected to a supply. Determine the current flowing in the conductor if the force on the conductor is measured at 2·4 N. **3**

[Turn over

11. (continued)

(*c*) For the circuit shown in Figure Q11(*c*) determine:

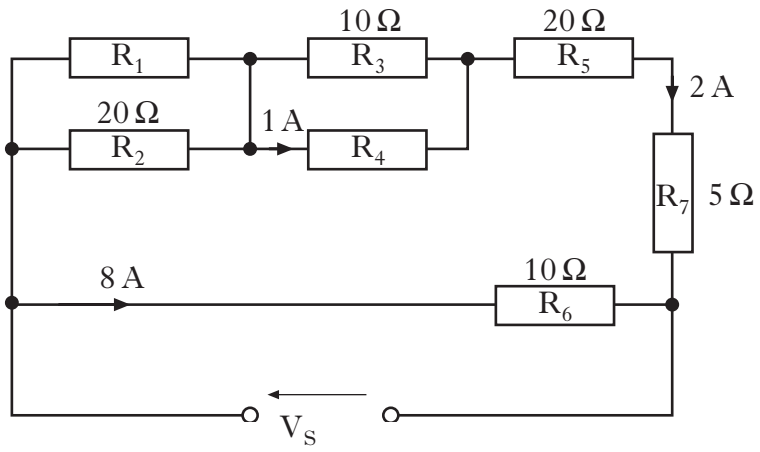


Figure Q11(*c*)

(i) the supply voltage V_S; **2**

(ii) the total circuit resistance; **2**

(iii) the current through resistor R_3; **1**

(iv) the voltage across resistor R_3; **1**

(v) the value of resistor R_4; **1**

(vi) the voltage across resistor R_1; **2**

(vii) the value of resistor R_1. **2**

(*d*) For the circuit shown in Figure Q11(*d*) determine:

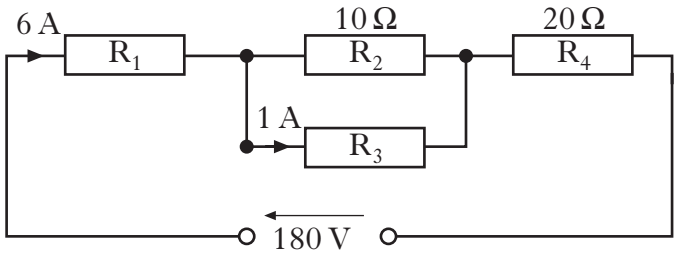


Figure Q11(*d*)

(i) the power dissipated in the 10 Ω resistor R_2; **2**

(ii) the total power dissipated in the circuit; **1**

(iii) the energy consumed, in Joules, if the circuit is operated for 2 hours. **2**

(25)

Marks

12. (*a*) Identify the circuit shown in Figure Q12(*a*) and identify the purpose of each of the capacitators C_1, C_2 and C_3. **4**

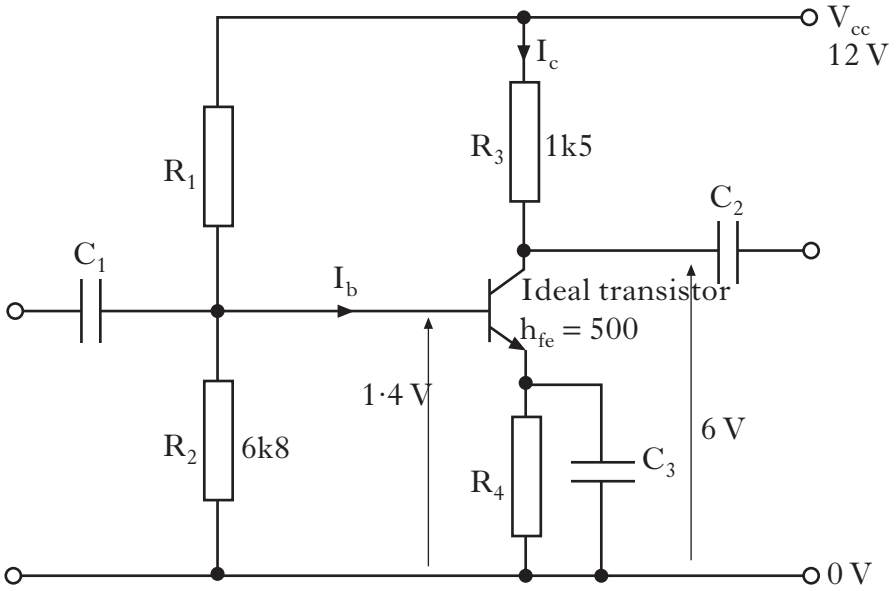


Figure Q12(*a*)

(*b*) For the circuit shown in Figure Q12(*a*) calculate:

(i) the collector current I_c; **2**

(ii) the base current I_b; **2**

(iii) the current through the resistor R_2; **2**

(iv) the value of the resistor R_1. **3**

[Turn over for Question 12(*c*) and (*d*) on *Page twelve*

12. (continued)

Marks

(*c*) For the circuit shown in Figure Q12(*c*).

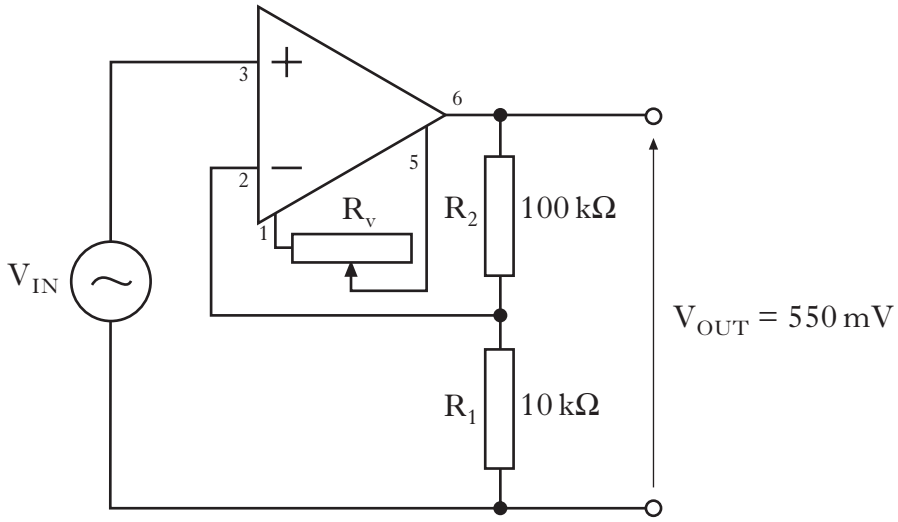


Figure Q12(*c*)

(i) Identify the circuit configuration shown in Figure Q12(*c*). **1**

(ii) Determine the gain of the circuit and the input voltage. **4**

(iii) When setting up the circuit it is found that for an input of 0 V the output is not zero.

A What component in Figure Q12(*c*) will allow the output to be adjusted to zero? **1**

B What is this process called? **2**

(*d*)

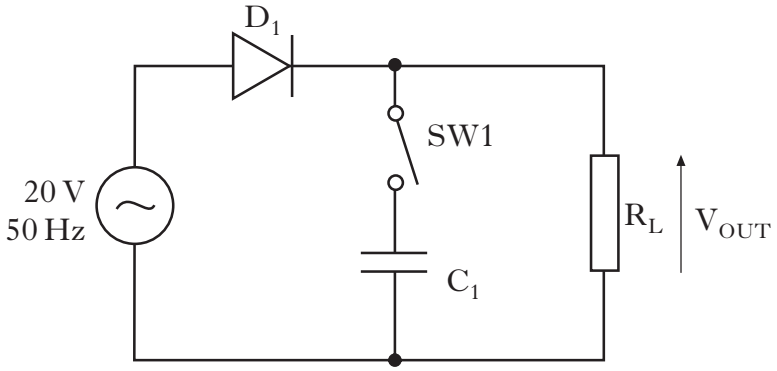


Figure Q12(*d*)

Sketch the output waveform for the circuit shown in Figure Q12(*d*) with

(i) SW1 open, and **2**

(ii) SW1 closed. **2**

(25)

[*END OF QUESTION PAPER*]

X025/202

NATIONAL QUALIFICATIONS 2011

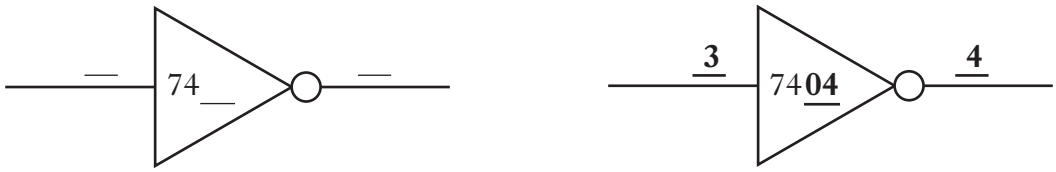
TUESDAY, 7 JUNE
1.00 PM – 3.30 PM

ELECTRONIC AND ELECTRICAL FUNDAMENTALS
INTERMEDIATE 2
Worksheet for Q10(*c*)

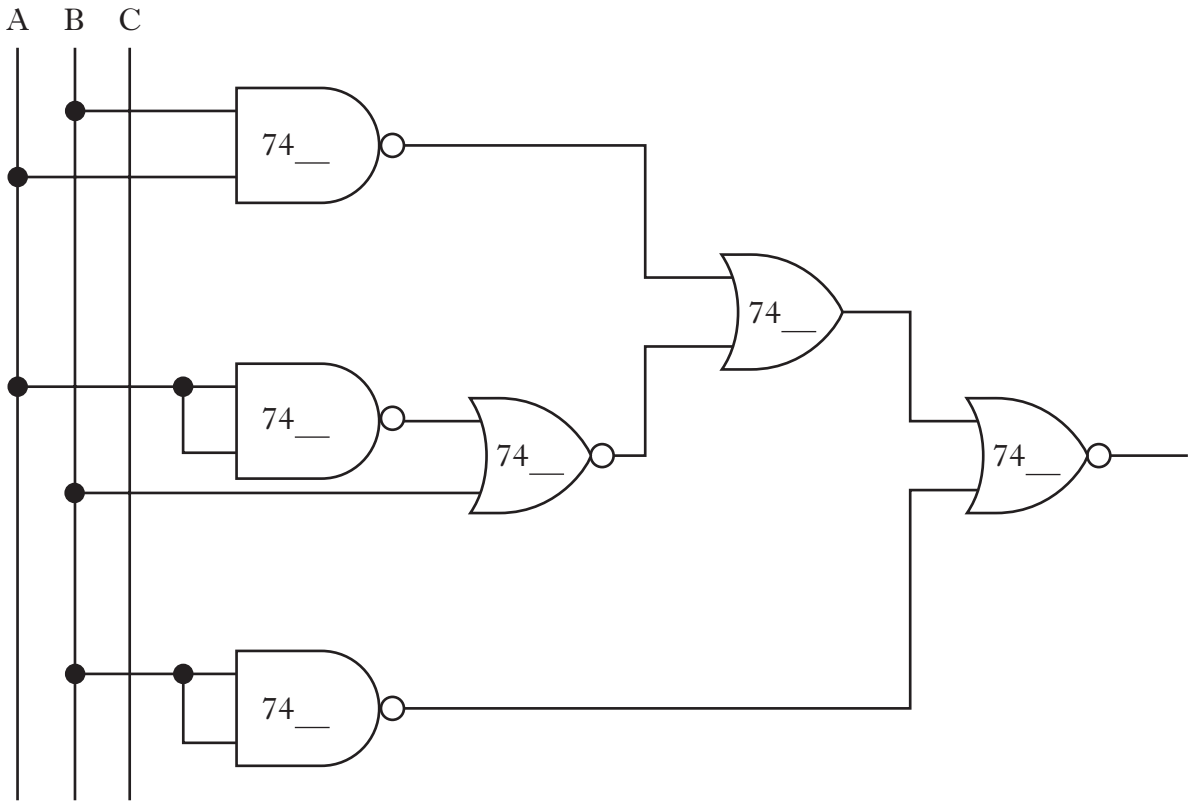
PB X025/202 6/310

Worksheet for Question 10(*c*)

Sample Solution



Refer to Datasheet



[*END OF WORKSHEET*]

X025/203

NATIONAL QUALIFICATIONS 2011

TUESDAY, 7 JUNE 1.00 PM – 3.30 PM

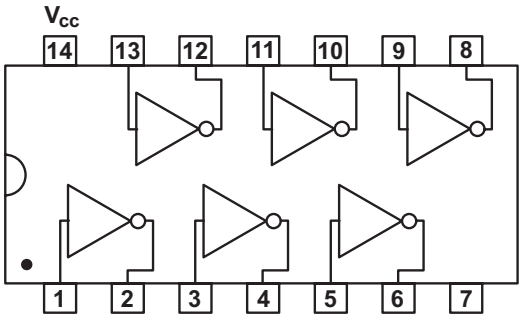
ELECTRONIC AND ELECTRICAL FUNDAMENTALS
INTERMEDIATE 2
Datasheet for Q10(*c*)

PB X025/203 6/310

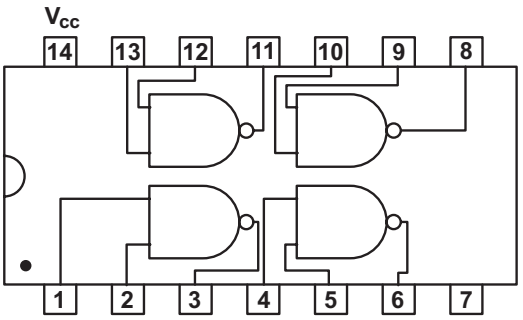
Datasheet for Question 10(*c*)

Logic Data sheet

Note: You may use any of the 6 logic chips and each logic chip may only be used once.



7404



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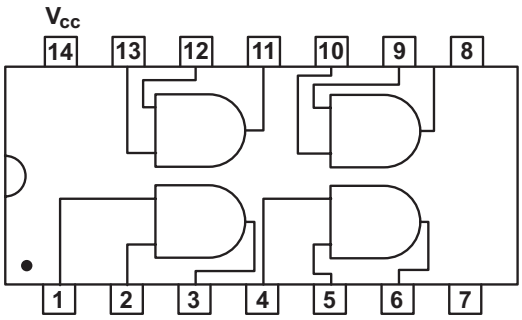
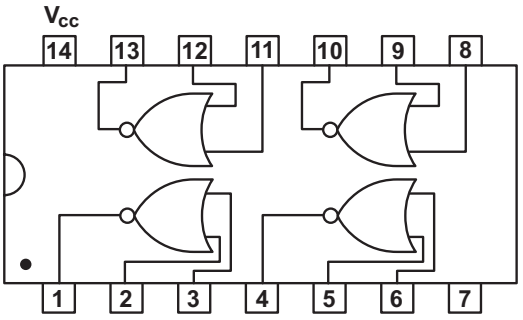
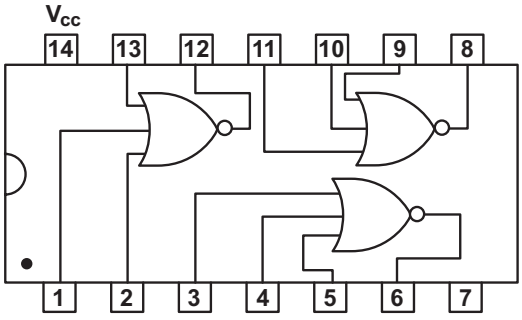


7408



7402



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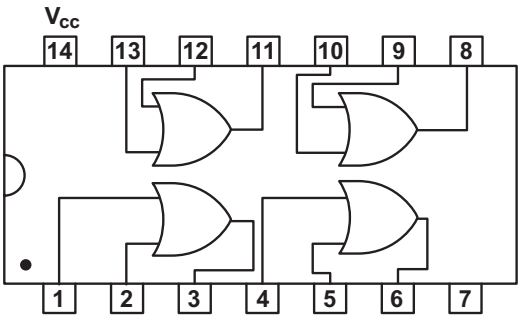

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[*END OF DATASHEET*]