

Q.1

a. Explain short channel effect in MOSFET.

Answer:

1. (a) The short channel effect is the decrease in MOSFET threshold voltage as the channel length is reduced. It is essentially pronounced when the drain is biased at a voltage equal to that of the power supply. In a CMOS VLSI technology, channel length varies statistically from chip to chip, wafer to wafer and lot to lot due to process tolerances. The short channel effect is therefore, an important consideration in device design. The threshold voltage should not become too low for minimum channel-length device on chip. The variation of threshold voltage of nMOSFET and pMOSFET versus channel length is shown below.



b. Describe molecular beam epitaxy method to grow crystal.

Answer:

(b) Molecular beam epitaxy (MBE) is a non chemical vapour deposition epitaxial process that uses an evaporation method. The essence of the method is an evaporation of silicon and one or more dopants, as described below.

The schematic diagram of an MBE growth system shows a cross-section of a vacuum chamber. At the top, there is a hot plate with a substrate holder. A quartz crystal thickness monitor is positioned to monitor the growing layer. A view port is located on the side. Inside the chamber, there is a mechanical shutter and an Sb effusion cell. At the bottom, there are two pumps: a titanium sublimation pump and a turbo molecular pump. On the left side, there is a mass spectrometer and an ionization gauge. An e-gun and Si source are also indicated at the bottom left. The entire system is surrounded by heat shielding.

Schematic of MBE growth system

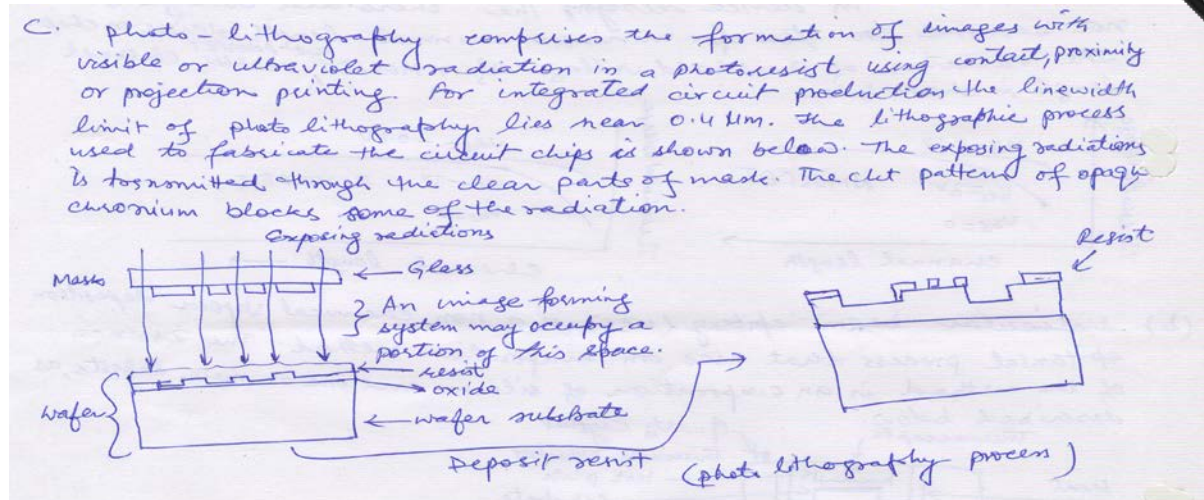
The evaporated species are transported at a relatively high velocity in vacuum to the substrate. The relative low vapour pressure of Si and the dopant ensures consideration at low temperature substrate. The Silicon MBE is performed under ^{ultra}high vacuum conditions of 10^{-8} to 10^{-10} torr. The mean free path of atoms is

$$L = 5 \times 10^3 / p.$$

Because of collision between atoms are unimportant in a high vacuum, the transport velocity is controlled by thermal energy effects than by diffusion effects. MBE doping has several features. A wider choice of dopants can be used, more control of doping profile is possible.

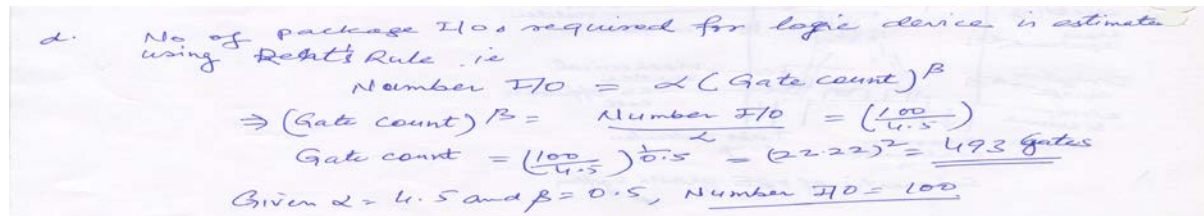
c. Explain photo-lithography process to fabricate circuit chips.

Answer:



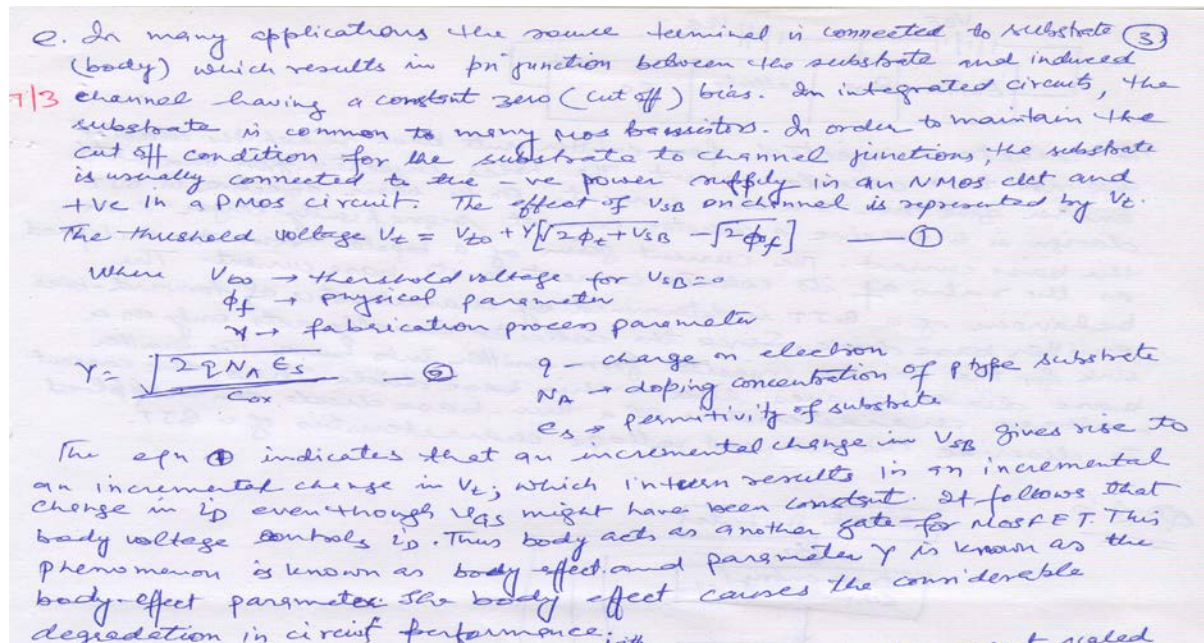
d. Estimate the number of gates that can be included on a logic – gate array chip which is to be assembled in a 100 I/O package. Assume $\alpha = 4.5$ and $\beta = 0.5$

Answer:



e. Explain body effect in MOSFET.

Answer:



f. Explain the effect of scaling on circuit parameters.

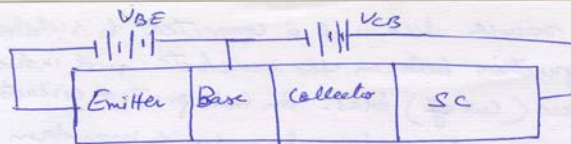
Answer:

degradation in circuit performance.
f. Effect of scaling on circuit parameters: - Both voltage and current scaled down by some factor, the active channel resistance of the scaled down device remains unchanged. It is further assumed that parasitic resistance is either negligible in scaling. The circuit delay, which is proportional to RC or CV/I then scales down by k . Thus, Once the device dimensions and power supply voltage are scaled down, the circuit speeds up by some factor. Moreover, power dissipation per circuit, which is proportional to V^2/R , is reduced by k^2 . Since the circuit density has increased by k^2 , the power density remains unchanged in the scaled down device. The power-delay product of scaled CMOS circuit shows a dramatic improvement by a factor of k^3 .

g. Explain two PN diode model of BJT.

Answer:

improvement by a factor of k^3 .
g. PN diode model of BJT: BJT consists of two PN diodes connected back to back. The basic operation of BJT can be described by operation back to back-diodes. To turn PNP transistor on the emitter base diode is forward biased, resulting in holes being injected from base into the emitter and electrons being injected from emitter into base. In normal operation, base-collector diode is reverse biased so that there is no forward current flow in the base-collector diode. The bias condition condition is shown below.

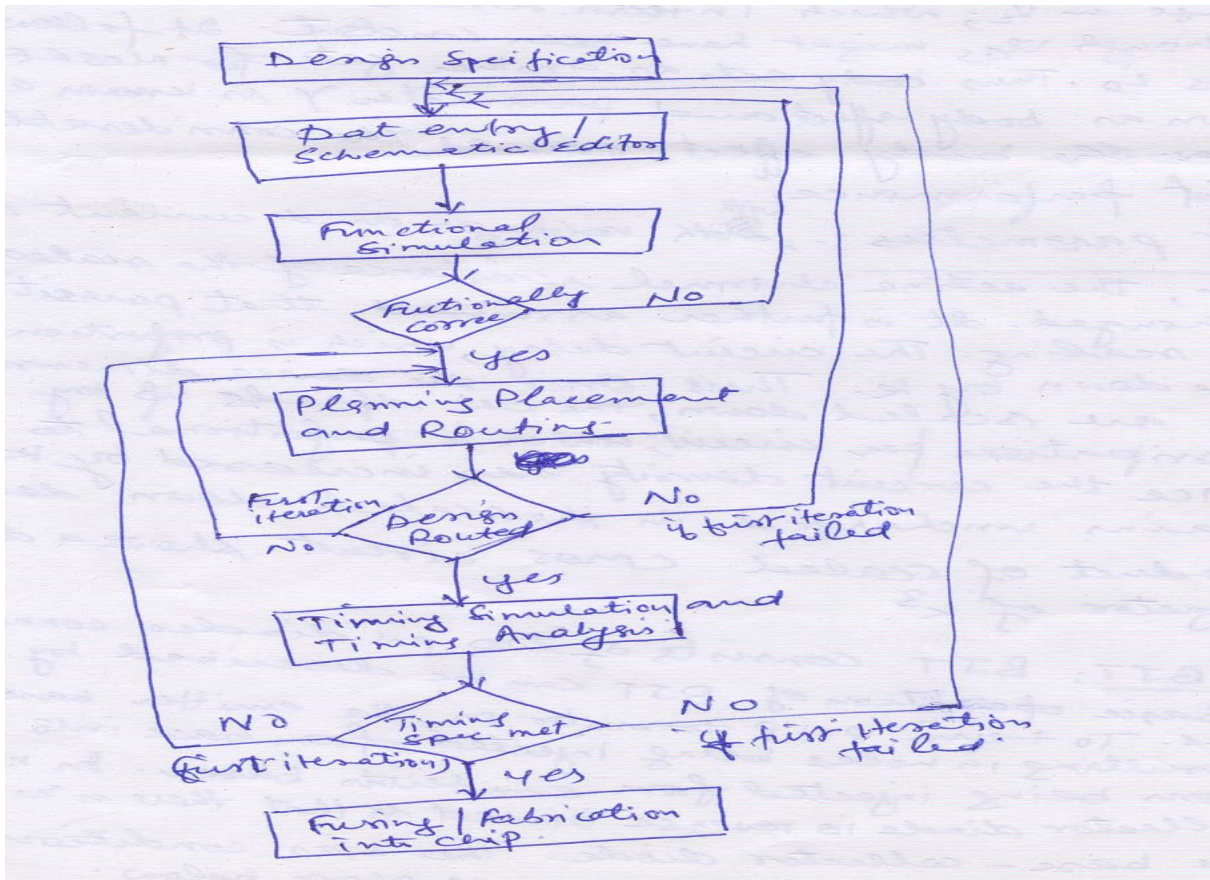


The electrons injected from emitter into base reach the collector, give rise to a collector current. The holes injected from base into emitter give rise to a base current. On the basic objective in BJT design is to achieve a collector current significantly larger than the base current. The current gain of a bipolar transistor is defined as the ratio of its collector current to its base current. The behaviour of a BJT is determined by characteristics of forward-bias emitter base diode, Since the collector usually acts only as a sink for the carrier injected from emitter into base. The emitter base diode behaves like a thin base diode. Thus the current-voltage characteristics of a thin-base diode can be applied to describe the current-voltage characteristics of a BJT.

Q.2

a. Explain VLSI design flow.

Answer:



b. Give the comparison between CMOS and bipolar technologies.

Answer:

(b) CMOS Technology

1. Low static power dissipation
2. High I/P impedance
3. Low drive current
4. Scalable threshold voltage
5. High noise margin
6. High packaging density
7. High delay sensitivity
8. Bidirectional capabilities
9. Low g_m ($g_m \propto V_{in}$)
10. Low op drive current

Bipolar Technology A17/3

1. High power dissipation
2. Low I/P impedance
3. High drive current
4. Scalable voltage
5. Low voltage swing logic
6. Low packaging density
7. Low delay sensitivity
8. Unidirectional
9. High g_m ($g_m \propto e^{V_{in}}$)
10. High op drive current

Q.3

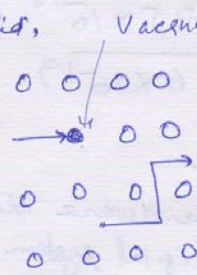
a. What is diffusion? Explain models of diffusion in solids.

Answer:

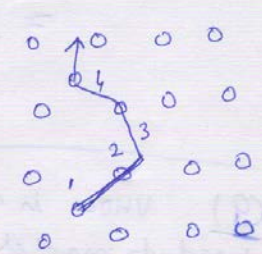
Q.3(a) Diffusion :- Diffusion means to alter the type of conductivity in silicon or germanium. This process of inducing dopant into silicon is known as diffusion.

Models of diffusion :- At high temperature, point defects such as vacancies and self interstitial atoms are generated in a single crystal solid. When the concentration gradient of the host atoms exists, such point defects affect atom movement. Diffusion in solids can be visualized as atomic movement of diffusion in the crystal lattice by vacancies. The fig below shows some common atomic diffusion models in a solid.

Using a simplified two dimensional crystal structure with lattice constant a . The open circles represent the host atoms occupying low temperature lattice positions.



(a)
Vacancy
Interstitial
mechanism



(b)
Interstitial
mechanism

An interstitial atom moving from one place to another place without occupying a lattice site is called interstitial diffusion mechanism. An atom smaller than host atom that does not form covalent bonds with silicon often moves interstitially. Fig (b) shows a 2 dimensional picture of the atomic movement of a self interstitial atom displacing an impurity atom, which in turn becomes an interstitial atom. Subsequently, the impurity atom displaces another host atom and the second host atom becomes a self interstitial. This is an example of extended interstitial mechanism. The vacancy and interstitially mechanisms are considered the doping mechanism for dopant impurity diffusion in silicon.

b. What is the stored charge and number of electrons on an MOS capacitor with an area of $4 \mu\text{m}^2$ a dielectric of $200 \text{ \AA}$ thick SiO_2 and applied voltage of 5V ?

Answer:

b. The charge $Q_s = C A \frac{V_s}{d}$
 $C = 3.9 \times 8.85 \times 10^{-14} \text{ F/cm}$, $A = 4 \times 10^{-8} \text{ cm}^2$
 $V_s = 5\text{V}$, $d = 2 \times 10^{-6} \text{ cm}$
 $\therefore Q_s = 3.9 \times 8.85 \times 10^{-14} \times 4 \times 10^{-8} \times \frac{5}{2 \times 10^{-6}}$
 $= 3.45 \times 10^{-14} \text{ C}$
 Charge on electron $= 1.6 \times 10^{-19} \text{ C}$
 $\therefore \text{No of electrons} = \frac{\text{Total Charge Stored}}{\text{Charge on one electron}}$
 $= \frac{3.45 \times 10^{-14}}{1.6 \times 10^{-19}} = 2.15 \times 10^5 \text{ electrons}$

Q.4

a. How VHDL is used to model the digital.

Answer:

Q.4 (a) VHDL is a hardware description language that is used to model a digital system. It provides five different types of primary constructs, called design units; they are

- Entity declaration
- Architecture body
- Configuration declaration
- Package declaration
- Package body

An entity is modeled using an entity declaration and at least one architecture body. The entity declaration describes the external view of the entity. The architectural body contains the internal description of the entity. For example, a set of interconnected components that represents the structure of the entity or as a set of concurrent or sequential statements that represents the behaviour of the entity. Each style of representation can be specified in a different architectural body or mixed within a single architectural body.

A configuration declaration is used to create a configuration for an entity. It specifies the binding of one architecture body from many architecture bodies that may be associated with the entity. It also specifies the bindings of components used in the selected architecture body to other entities. An entity may have any number of different configurations.

A package declaration encapsulates a set of related declarations such as type declarations, subtype declarations and subprogram declarations which can be shared across two or more design units.

A package body contains the definitions of subprograms declared in a package declaration.

... the OP not only depend on the state of finite state ...

b. Give state transition table for Mealy machine.

Answer:

units.
A package body contains the design in a package declaration.

b. In a Mealy finite machine the o/p not only depend on the state of the machine but also on its inputs. This type of finite state machine can also be modeled in a style similar to that of the Moore machine. The state transition table for Mealy machine

	0	1
ST0	ST0 / 0	ST3 / 1
ST1	ST1 / 1	ST0 / 0
ST2	ST2 / 0	ST1 / 1
ST3	ST2 / 0	ST1 / 0

Q.5

a. Draw the block diagram of a general two-stage op-amp and explain the working operation of each block.

Answer:

Q5a. The fig below shows the inverter. It performs logic operation

When the input of inverter is connected to ground, the o/p is pulled to V_{DD} through p-channel transistor. When the I/P terminal is connected to V_{DD} , the o/p is pulled to ground through the n-channel MOSFET.

DC characteristics:

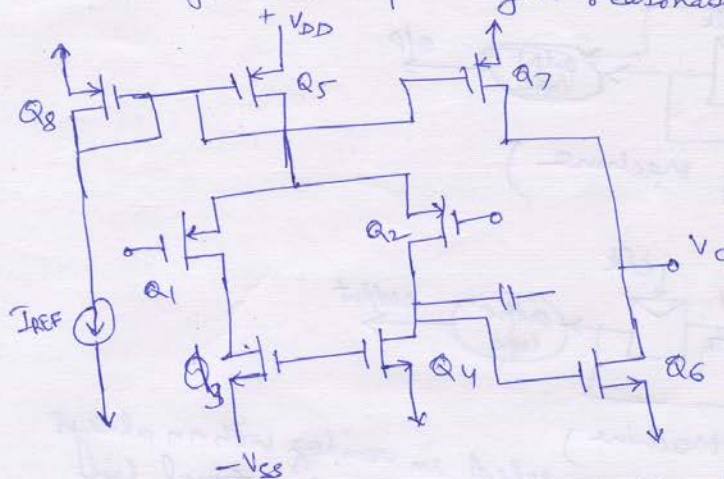
In region 1 of transfer characteristics, the I/P voltage is sufficiently low so that M_1 is off and M_2 is on. As V_{in} is increased, both M_2 and M_1 turn on. Increasing V_{in} further causes M_2 to turn off and M_1 to turn on fully (Region 3).

The maximum o/p high voltage is labeled V_{OH} and minimum o/p low voltage V_{OL} . Points A and B on this curve are defined by the slope of the transfer curve. The I/P voltage less than V_{IL} defined by point A are considered as logic low on input of the inverter. Input voltage greater than or equal to V_{IH} defined by point B are considered as logic high on the I/P of inverter. Input voltage between V_{IL} and V_{IH} do not define a valid logic voltage level.

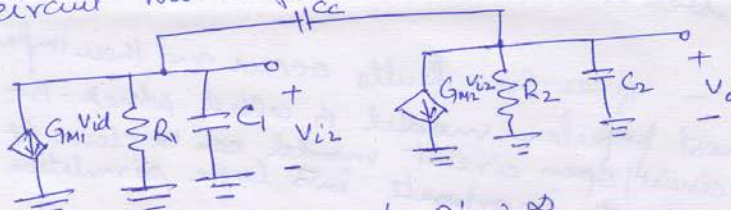
b. Draw the two stage CMOS OPAMP Configuration and calculate its voltage gain.

Answer:

b. the circuit consists of two gain stages. The first stage is formed by differential pair $Q_1 - Q_2$ together with its current mirror load $Q_3 - Q_4$. The differential amplifier circuit provides a voltage gain as well as perform conversion from differential to single ended form while providing a reasonable CMRR.



To determine the voltage gain, consider a simplified equivalent circuit model for small signal operation of CMOS amplifier.



Input resistance is infinite $R_{in} \rightarrow \infty$
 First stage transconductance G_{m1} is = transconductance of each g_{m1} and g_{m2} i.e. $G_{m1} = g_{m1} = g_{m2}$

$$G_{m1} = \frac{2(I/2)}{V_{ov1}} = \frac{1}{V_{ov1}} \quad (1)$$

$$R_1 = R_{o2} \parallel R_{o4} \quad (2)$$

$$R_{o2} = \frac{|V_{A2}|}{I/2} \quad (3)$$

$$R_{o4} = \frac{V_{A4}}{I/2} \quad (4)$$

$$\begin{aligned} A_1 &= -G_{m1} R_1 \\ &= -g_{m1} (R_{o2} \parallel R_{o4}) \\ &= -\frac{2}{V_{ov1}} \left(\frac{1}{V_{A2}} + \frac{1}{V_{A4}} \right) \quad (5) \end{aligned}$$

$$G_{m2} = g_{m6} = \frac{2I_{D6}}{V_{ov6}} \quad (6)$$

$$R_2 = R_{o6} \parallel R_{o7}$$

$$R_{o6} = \frac{V_{A6}}{I_{D6}}$$

$$R_{o7} = \frac{|V_{A7}|}{I_{D7}} = \frac{|V_{A7}|}{I_{D6}} \quad (7)$$

$$A_2 = -G_{m2} R_2 = -\frac{2}{V_{ov6}} \left(\frac{1}{V_{A6}} + \frac{1}{V_{A7}} \right) \quad (8)$$

Voltage gain

$$A_v = A_1 A_2 = G_{m1} R_1 G_{m2} R_2$$

$$= g_{m1} (R_{o2} \parallel R_{o4}) g_{m6} (R_{o6} \parallel R_{o7}) \quad (9)$$

Q.6

a. Explain finite state machines.

Answer:

Q.6a Finite State Machine: There are two styles of finite state machines. In Mealy machines, the OP is a function of the current state and inputs. In the Moore machine, the OP is a function of only the current state.

(Mealy machine)

(Moore machine)

Finite state machines are modelled in verilog with an always block defining the state registers and combinational logic defining the next state and OP logic.

b. Explain fault model in VLSI design.

Answer:

defining the next state

b. Fault Models:- gives how faults occur and their impact on circuits. The most popular model is called stuck-at model. The short circuit/open circuit model can be closer fit to reality, but is harder to incorporate into logic simulation tools.

(i) Stuck at Faults Model: In this model, a fault gate input is modelled at stuck at zero or stuck at one. This model dates from board-level designs, where it was determined to be adequate for modelling faults. These faults most frequently occur due to gate oxide shorts or metal to metal shorts. Fig 1 below

(ii) Short circuit / Open circuit faults includes stuck-open or shorted models. The shorted results in an S-A-0 fault at point A, while short S2 modifies the function of gate. It is evident that to ensure the most accurate modeling fault should be modelled at transistor level because it is only at this level that the complete ckt structure is known. Fig 2 below

Fig 1

Fig 2

Q.7

a. Explain the importance of scaling of MOS transistor dimensions. Explain the types of scaling and show the effects of parameters in constant voltage scaling.

Answer:

Q.7 a. MOSFET capacitance: consider the crosssectional view of (7)

The capacitance between gate electrode and substrate electrode is

$$C_{gb} = \frac{\epsilon_{ox} (L - 2L_D) W}{T_{ox}}$$

Where $\epsilon_{ox} \rightarrow$ dielectric constant
 $L - 2L_D \rightarrow$ effective channel length
 $W \rightarrow$ width

The capacitance between gate and the source/drain is simply the overlap capacitance. As we increase V_{GS} , a capacitance between gate and induced channel under oxide layer exists this capacitor is known as depletion capacitance.

When V_{GS} is sufficiently large so that a large no. of electrons are attracted under gate, the surface is said to be inverted i.e. no longer p-type. Thus the capacitance from gate to ground changes as V_{GS} changes for MOSFET configuration. The following capacitance exists in MOSFET

- $C_{gb} \rightarrow$ capacitance associated with gate poly over field region
- $C_{gd} \rightarrow$ drain capacitance
- $C_{gs} \rightarrow$ gate source capacitance

5. (1) Scaling of MOS transistor dimensions

MOS technology evolution in the past twenty years has followed the path of device scaling for achieving density, speed and power improvement. MOSFET scaling was propelled by rapid advancement of lithographic techniques for delineating fine lines of 1 μm width and below. Reducing the source to drain spacing i.e. channel length of MOSFET led to short channel effects. Another necessary technology advancement for device scaling is in ion implantation, which is not only allows the formation of very shallow source and drain region but also capacitance of accurately introducing a sharply profiled, low concentration of doping atoms for optimum channel profile design. Scaling can be

- Constant field scaling.
- Generalized scaling.
- Constant voltage scaling.