ROLL NO. _____

**Code: DE58/DC58** **Subject: LOGIC DESIG**

## DipIETE – ET/CS

**Time: 3 Hours** **DECEMBER 2013** **Max. Marks: 100**

***PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.***

**NOTE: There are 9 Questions in all.**

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

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**Q.1 Choose the correct or the best alternative in the following:** **(2×10)**

a. A memory that requires refreshing is _____

**(A)** ROM **(B)** SRAM
**(C)** DRAM **(D)** Flash RAM

b. The hexadecimal representation of 177 is _____

**(A)** 112 **(B)** B1
**(C)** 111 **(D)** 2D

c. BCD code 11001011 represents the decimal number _____

**(A)** 190 **(B)** 203
**(C)** 52 **(D)** 5

d. The sum of product of $(x + y' + c)(x' + y' + c)$ is _____

**(A)** $y' + c$ **(B)** $xy' + cx'$
**(C)** $y' + xc$ **(D)** $x'y + y'c$

e. Two RS flipflops connected sequentially with complementary clocks forms a _____

**(A)** two bit shift register **(B)** two bit counter
**(C)** JK flip flop **(D)** MS flip flop

f. A 8 bit synchronous counter using flip-flops each of propagation delay 12 nsec and gate delay of 8nsec, provides a transition delay of _____

**(A)** 68nsec **(B)** 104nsec
**(C)** 20nsec **(D)** 48nsec

g. A parallel binary adder can be made faster by

**(A)** using serial adder configuration **(B)** gated input configuration
**(C)** carry look ahead configuration **(D)** complementary addition system

h. A three bit counter divides the clock by_____

**(A)** 3 **(B)** 7
**(C)** 8 **(D)** 2

i. Johnson counter is realized using a _____

**(A)** Ripple Counter **(B)** Serial Adder
**(C)** Multiplexer **(D)** Shift Register

j. Parallel to serial conversion requires_____

**(A)** Counter **(B)** Multiplexer
**(C)** Shift Register **(D)** Decoder

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**Answer any FIVE Questions out of EIGHT Questions.**
**Each question carries 16 marks.**

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**Q.2** a. Perform the following conversions: **(6)**

(i) $(2496)_{10} = (?)_8$

(ii) $(CF3D)_{16} = (?)_{10}$

(iii) $(11011.0111)_2 = (?)_{10}$

b. Draw the functional diagram of a digital computer and explain the function of each block. **(6)**

c. Give examples of parallel and serial transmission in digital systems. **(4)**

**Q.3** a. What is the need to minimize a Boolean expression? What are the methods used to achieve these. **(4)**

b. Minimize the following Boolean expressions and write the truth tables to show that the minimized expressions will produce the same output as the expanded expressions. **(12)**

(i) $F = m_0 + m_2 + m_5 + m_7 + m_8 + m_{10} + m_{13} + m_{15}$

(ii) $y = (A' + B)(A' + B + D)(C + D')$

**Q.4** a. Draw the logic diagram of eight bit serial in/parallel out shift register and explain its operation. **(8)**

b. What is meant by multiplexer? List out its various applications. **(4)**

c. Explain briefly with the help of waveforms, how propagation delay occurs in Ripple Counters? **(4)**

**Q.5** a. Distinguish between asynchronous and synchronous Flip Flops. Convert an asynchronous RS flip flop into synchronous latch. **(6)**

b. Design a decade counter using JK Flip Flops and draw its timing diagram. **(6)**

c. What is the need of Schmitt trigger devices, explain with waveforms. **(4)**

**Q.6** a. Build a Full Adder using two Half Adders and prove that the addition of two numbers results in subtraction when 2's complement is used. **(8)**

b. If a single bit Full Adder takes 8sec for addition, calculate the total addition time taken to add two numbers having hundredth weight. Suggest a method of speeding up the addition. **(8)**

**Q.7** a. Design a seven segment decoder that is required to drive an active low seven segment display. **(8)**

b. What are the advantages and disadvantages of a synchronous counter over an asynchronous counter? **(4)**

c. How many AND gates are required to decode completely all of the states of a MOD-32 binary counter? What are the inputs to the gate that decodes for the count of 21? **(4)**

**Q.8** a. How will you read and write into a 16×4 RAM? Draw a schematic of this RAM and explain the process. **(8)**

b. Design a mod 7 synchronous counter and calculate its maximum frequency of operation if the flip flop delay time is 8nano sec. and gate delay time is 5nano sec. **(8)**

**Q.9** Explain the principle of the following: **(4×4)**

(i) Magnitude Comparator
(ii) CPU and memory interface
(iii) Johnson Counter
(iv) DRAM