ROLL NO. _____

Code: AE74 **Subject: VLSI DESIGN**

AMIETE – ET

Time: 3 Hours **DECEMBER 2013** **Max. Marks: 10**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The threshold voltage of n-MOS depletion mode transistor when $V_{SB} = 0$ is

(A) $V_{td} = +0.2V_{DD}$ **(B)** $V_{td} = -0.7V_{DD}$
(C) $V_{td} = -0.2V_{DD}$ **(D)** $V_{td} = +0.7V_{DD}$

b. The total number of transistors required to realize 3-input n-MOS NAND gate is

(A) 2 **(B)** 3
(C) 4 **(D)** 6

c. If $V_{tn} = +0.55V$ and $V_{in} = 2.9$ V, then the output voltage (V_{out}) of the two n-FET chain shown in **Fig.1** is

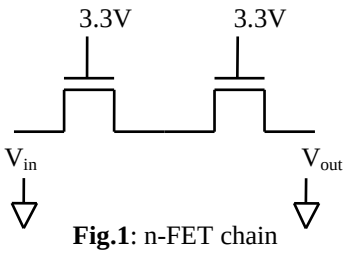

Fig.1: n-FET chain

(A) 2.75V **(B)** 2.9V
(C) 3.3V **(D)** 0V

d. In n-MOS design rules the minimum separation between diffusion to diffusion is

(A) 1λ **(B)** 2λ
(C) 3λ **(D)** 4λ

e. In 5 μm technology, the value of standard unit of capacitance is

(A) 0.1 PF **(B)** 0.0023 PF
(C) 0.0032 PF **(D)** 0.01 PF

f. The condition to work n-MOS transistor in saturation region

(A) $V_{gs}>V_t$ & $V_{ds}<V_{gs}-V_t$ **(B)** $V_{gs}<V_t$ & $V_{ds}>V_{gs}-V_t$
(C) $V_{gs}>V_t$ & $V_{ds}>V_{gs}-V_t$ **(D)** $V_{gs}>V_t$ & $V_{ds}=0$

g. The Z_{pu}/Z_{pd} ratio of Pseudo n-MOS inverter driven through similar inverter is

(A) 3/1 **(B)** 1/3
(C) 4/1 **(D)** 1/4

h. The dynamic power consumption (P_d) of a CMOS is given by

(A) $m(C_L V^2_{DD} f)$ **(B)** $V^2_{DD} f$
(C) $V^2_{DD} T$ **(D)** $V_{DD} f$

i. The High level noise margin (NM_H) of inverter is given by

(A) $V_{IH}-V_{IL}$ **(B)** $V_{OH\ min}-V_{IL\ min}$
(C) $V_{OH\ max}-V_{OL\ max}$ **(D)** $V_{IH\ max}-V_{IL\ max}$

j. The objective of Built in Self Test (BIST) is to

(A) Reduce test pattern generation cost **(B)** Reduce the value of test data
(C) Reduce test time **(D)** All of these

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain with sketches P-well process of CMOS fabrication. **(8)**

b. What is the importance of Twin-Tub process? Sketch cross-sectional view of Twin-Tub Inverter. **(5)**

c. Mention the advantages of CMOS over Bipolar technology. **(3)**

Q.3 a. Starting from the fundamentals derive an expression for I_{ds} of n-MOS inverter in saturation region and linear region**.** **(7)**

b. What is Latch-up in CMOS? Sketch latch-up circuit for CMOS n-well process. **(5)**

c. For n-MOS enhancement transistor, μ_n = 215 cm^2/Vsec, Oxide capacitance (Cox) = 2.3 fF/ μm^2, drain current (I_d) = 100 μA and W/L = 10. Calculate Transconductance (g_m). **(4)**

Q.4 a. Discuss λ-based design rules for wires and contacts. **(8)**

b. Draw stick-diagrams for n-MOS inverter, P-well CMOS inverter **(8)**
(i) 3-input n-MOS NOR gate
(ii) 2-input CMOS (P-well) NOR gate

Q.5 a. Show that the total delay of cascaded N number of CMOS inverters is $3.5\,eN\tau$. **(7)**

b. Explain how Super buffers can be used to achieve symmetrical transitions, when inverters are used to drive more capacitive loads. **(5)**

c. Find the time constant (τ_p) of p-FET for the following parameters:
$(W/L)_p = 8$, $K_p = 62\ \mu A/V^2$, $V_{tp} = -0.85$ V, $V_{DD} = 3.3$ V, the total capacitance is 150 fF. **(4)**

Q.6 a. Write the scaling factors for the following device parameters. **(8)**

(i) Gate capacitance
(ii) Saturation current I_{dss}
(iii) Power speed product (P_T)

b. With truth table and stick diagram explain Bus arbitration logic for n-line bus. **(8)**

Q.7 a. Explain the operation of 4x4 barrel shifter with schematic. What is the limitation of 4x4 crossbar switch? **(8)**

b. Design a single bit adder and implement 4-bit ALU functions using adder elements. **(8)**

Q.8 a. Explain with circuit diagram n-MOS and CMOS Pseudo-static memory cells. **(8)**

b. Discuss briefly the ground rules for successful design. **(8)**

Q.9 Write short notes on : **(4×4=16)**

(i) Design style and philosophy
(ii) System partitioning
(iii) Boundary Scan Test (BST)
(iv) Built-In-Self-Test (BIST)