ROLL NO. _____

Code: AE68 **Subject: EMBEDDED SYSTEMS D**

AMIETE – ET

Time: 3 Hours **DECEMBER 2013** **Max. Marks: 10**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. A _____ tool converts a sequential program into finite state machines and register transfer logic.

(A) RT synthesis **(B)** logic synthesis
(C) behavioral synthesis **(D)** system synthesis

b. The programs that run on the development processor but execute code designed for the target processor is known as _____.

(A) instruction set simulator **(B)** cross compilers
(C) device programmer **(D)** ASIPs

c. The resolution of ADC/DAC is expressed as _____, where V_{max} is the maximum voltage of the analog signal and n is the number of bits for digital encoding.

(A) $V_{min} / (2^n + 1)$ **(B)** $V_{min} / (2^n - 1)$
(C) $V_{max} / (2^n - 1)$ **(D)** $V_{max} / (2^n + 1)$

d. Identify the false statement from the following:

(A) cache is more expensive and faster than main memory
(B) cache is slower than main memory
(C) cache is designed using static RAM
(D) cache appears on the same chip as a processor

e. In Direct Memory Access, the purpose of _____ is to transfer data between memories and peripherals.

(A) Semaphore **(B)** ISR
(C) Pipes **(D)** DMA controller

f. In a _____ protocol, the master uses one control line, often called the _____ line, to initiate the data transfer.

(A) handshake, acknowledge **(B)** strobe, handshake
(C) strobe, request **(D)** handshake, request

g. If one task is running and another higher priority task unblocks, then the task that is running gets stopped and moves to the ready state. This is a feature of _____.

(A) Non-preemptive RTOS **(B)** Preemptive RTOS
(C) Jump RTOS **(D)** Prioritized RTOS

h. In _____, the stored bits are susceptible to undesired changes if the chip is used in environments with much electrical noise or radiation.

(A) OTP ROM **(B)** PROM
(C) EEPROM **(D)** EPROM

i. Embedded system microcontrollers use sleep mode and idle mode to

(A) save power **(B)** save memory
(C) save cpu **(D)** save i/p

j. Most RTOS maintain a _____ that interrupts periodically and used for all RTOS timing services.

(A) heartbeat timer **(B)** system timer
(C) embedded timer **(D)** logical timer

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Mention design metrics of an embedded system. Differentiate the following:
(i) General-purpose processors
(ii) Single purpose processors
(iii) Application-specific processors **(2+6)**

b. Give the sequence of steps to optimize the datapath and FSM in custom single purpose processors. **(5)**

c. Mention RTL sequential and combinational components.

Q.3 a. Explain various stages of instruction execution in a microprocessor. Give an illustration for non-pipelined and pipelined instruction execution. **(4+4)**

b. Explain the significance of FSMD in simple general purpose microprocessor with the help of diagram. **(5)**

c. Mention features of Digital Signal Processors (DSP) as ASIPs. **(3)**

Q.4 a. Explain the working of Pulse Width Modulators (PWM). Give the calculations for 25%, 50% and 75% duty cycles in PWM. **(3+3)**

b. For an analog output signal whose voltage range is from 0 to 10 V and an 5-bit digital encoding, calculate the encodings for :
(i) 2.25 V (ii) 5.75 V
(iii) 7 V **(6)**

c. Explain briefly the working of real-time clock in an embedding system. **(4)**

Q.5 a. Compare the following and give their respective applications:
(i) ROM (ii) Mask ROM
(iii) One-time Programmable ROM **(6)**

b. Give the block diagram of 4 × 4 RAM. Draw the memory cell internals for SRAM and DRAM. **(2+4)**

c. Explain any two cache mapping techniques. **(4)**

Q.6 a. Draw the transition diagram for task states. **(3)**

b. Define reentrancy. Mention three rules to decide if a function is reentrant. **(2+3)**

c. How do semaphores address the problems like priority inversion and the deadly embrace? Give an example for illustration. **(8)**

Q.7 Write short notes on any **FOUR** of the following:

(i) Strobe and handshake protocols
(ii) Memory mapped I/O and standard I/O
(iii) Multi-level bus architecture
(iv) I^2C serial protocol and PCI bus parallel protocol
(v) Wireless Protocols (IrDA, Blue Tooth and IEEE 802.11) **(4×4)**

Q.8 a. Explain the interrupt routine in RTOS. Give the working of interrupts for ISR, RTOS, TaskHigh and TaskLow. **(6)**

b. Explain the role of message queues, mailbox and pipes in RT interprocess communication. Give their respective advantages and disadvantages. **(6)**

c. Explain the role to timer function and events in RTOS. Give an example for illustration. **(4)**

Q.9 a. Explain the features of hard real-time scheduling and soft real-time scheduling. Give an example for illustration. **(6)**

b. Mention any four power saving techniques in RTOS. **(4)**

c. Design an application to illustrate RTOS. Give the block diagram and label various design components of RTOS. **(6)**