ROLL NO. ___________________

Code: AE54/AC54/AT54 Subject: LINEAR ICs & DIGITAL ELECTRONICS

AMIETE – ET/CS/IT

Time: 3 Hours **DECEMBER 2013** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part, each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. Karnaugh Map uses ________

(A) Binary Code **(B)** Grey Code
(C) BDC Code **(D)** Both **(A)** and **(B)**

b. For impedance matching application, OP-AMP is used as a ___________

(A) Voltage Follower **(B)** Voltage Clamper
(C) Voltage Clipper **(D)** Voltage Multiplier

c. An Integrated Circuit which consists of $10^6 - 10^7$ transistors / chip is called as ___________

(A) Medium Scale Integration **(B)** Large Scale Integration
(C) Very Large Scale Integration **(D)** Ultra Large Scale Integration

d. The output voltage (V_o) for the OP-AMP circuit of Fig.1 is _______

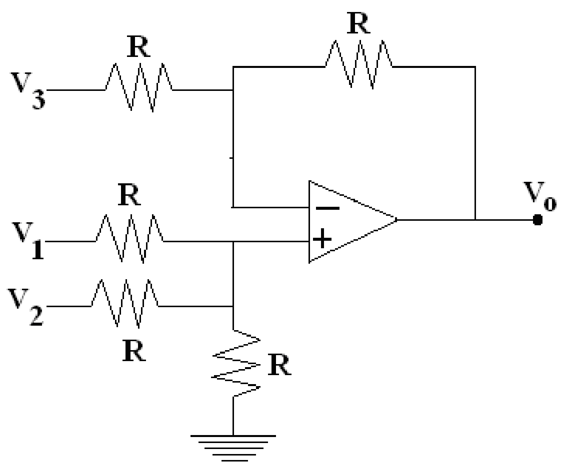

Fig. 1

(A) Vo = $V_3 - (V_1 + V_2)$
(B) Vo = $V_3 + (V_1 + V_2)$
(C) Vo = $-V_3 + (V_1 + V_2)$
(D) Vo = $-V_3 - (V_1 + V_2)$

e. For which of the following flip-flops, the output is clearly defined for all the combinations of two inputs _________

(A) D type flip-flop **(B)** R-S flip-flop
(C) J-K flip-flop **(D)** None of these

f. For the circuit of Fig.2, the input resistance R_{id} will be ____________

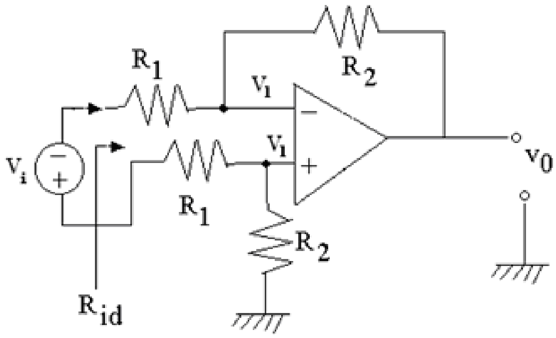

Fig.2

(A) $2R_1$ **(B)** $2R_1 + R_2$
(C) $2(R_1 + R_2)$ **(D)** Infinity

g. The number of states in its counting sequence that a Ring Counter consisting of 'n' flip-flops is ______

(A) $+2^{n-1}$ **(B)** 2^{n+1}
(C) n **(D)** n-1

h. A one-to-sixteen demultiplexer requires ________

(A) 2 select input lines **(B)** 3 select input lines
(C) 8 select input lines **(D)** 4 select input lines

i. The A/D converter which has maximum speed of conversion is _________

(A) Successive-approximation A/D converter
(B) Parallel-comparative A/D converter
(C) Counter ramp A/D converter
(D) Dual-slope A/D converter

j. Boolean Algebra states that the "OR ing of several variables results in the same regardless of the grouping of the variables" is called ___________

(A) Commutative Property **(B)** Associative Property
(C) Distributive Property **(D)** All of these

PART (A)
Answer At least TWO questions. Each question carries 16 marks.

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Q.2 a. Enlist the various advantages of IC over discrete component circuits. **(4)**

b. Draw basic differential amplifier and discuss transfer characteristics of an ideal operational amplifier. **(8)**

c. Design an amplifier with a gain of +5 using one OP-AMP **(4)**

Q.3 a. State non-ideal DC characteristics of an op-amp. Explain any two of them in detail. **(8)**

b. (i) Define Slew Rate of an op-amp
(ii) What causes the Slew Rate
(iii) How Slew Rate is measured
(iv) Can IC 741C be used for high frequency application? **(4×2)**

Q.4 a. Draw the characteristics of an ideal comparator and that of a commercially available comparator. Also list different types of comparators. **(6)**

b. Explain the following in detail using OP-AMP, assuming 1-V peak to peak square wave as input signal for
(i) Positive clipper (ii) Negative Clamper **(2×4)**

c. State the applications of a precision diode. **(2)**

Q.5 a. Describe the operation of an Astable multivibrator using 555 timer. **(8)**

b. Calculate the values of LSB, MSB and full scale output for an 8-bit DAC for the 0 to 10V range. **(6)**

c. What is a voltage regulator? State only name of the circuits that are used to make a regulated power supply. **(2)**

PART (B)
Answer At least TWO questions. Each question carries 16 marks.

Q.6 a. Differentiate between positive logic and negative logic. **(4)**

b. Perform the following conversions:
(i) $(110011011001)_2 = (\_\_\_\_)_{10}$ (ii) $(268)_{10} = (\_\_\_\_)_{16}$
(iii) $(39.12)_{10} = (\_\_\_\_)_2$ (iv) $(1054)_8 = (\_\_\_\_)_{10}$
(v) $(2040.125)_{10} = (\_\_\_\_)_{16}$ (vi) $(1001101.1011)_2 = (\_\_\_\_)_8$ **(6×2)**

Q.7 a. Why NAND and NOR gates are called universal gates? **(6)**

b. Prove that the given identity $Y = \overline{A + B}$ represents a NOR logic. **(4)**

c. (i) Draw the logic circuit for the given identity $Y = ABC + \overline{ABC} + B$
(ii) Simplify the expression and draw a logic circuit for the same. **(2×3)**

Q.8 a. What is Priority encoder? Draw & explain the truth table of decimal to BCD priority encoder. **(8)**

b. Design a Full Adder Circuit consisting of three inputs A, B, C_{IN} and two outputs S, C_{OUT} . **(8)**

Q.9 a. Write short notes on:-
(i) NAND gate latch (ii) Clocked D FF **(2×4)**

b. If data 1101 is fed into 4 bit Serial In / Serial Out Shift Register, show the status of register at various clock pulses. **(6)**

c. State one advantage and one disadvantage of synchronous counter over asynchronous counter. **(2)**