Code: AE05   **Subject: BASIC ELECTRONICS**

AMIETE – CS/IT (OLD SCHEME)

Time: 3 Hours   **JUNE 2012**   **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1   **Choose the correct or best alternative in the following:**   **(2×10)**

a. The intersection of a V-I curve with the load line is called the

   (A) Transfer curve   **(B)** transition point
   (C) Load point   **(D)** Q-point

b. If a single diode in a center tapped full-wave rectifier opens, the output is

   (A) 0 V   **(B)** half wave rectified
   (C) Reduced in amplitude   **(D)** unaffected

c. The purpose of a small capacitor placed across the output of an IC regulator is to

   (A) Improve transient response
   (B) couple the output signal to the load
   (C) Filter the ac
   (D) protect the IC regulator

d. When the collector resistor in a CE amplifier is increased in value, the voltage gain

   (A) Increases   **(B)** decreases
   (C) Is not affected   **(D)** becomes erratic

e. A type of transistor that is normally ON when the gate to source voltage is zero is

   (A) JFET   **(B)** D-MOSFET
   (C) E-MOSFET   **(D)** ALL of them.

f. Cross over distortion is a problem for

   (A) Class A amplifiers   **(B)** Class AB amplifiers

g. The output of a particular op-amp increases 8V in 12μs the slew rate is

    (A) 96 V/μs   **(B)** 0.67 V/μs
    (C) 1.5 V/μs   **(D)** none of these.

h. In Integrator, the feedback element is a

    (A) Resistor   **(B)** Capacitor
    (C) Diode   **(D)** Inductor

i. Wein-bridge oscillations are based on

    (A) Positive feedback   **(B)** negative feedback
    (C) The piezoelectric effect   **(D)** high gain

j. In a basic series regulator, V_{OUT} is determined by

    (A) the control element   **(B)** the sample circuit
    (C) the reference voltage   **(D)** answers **(B)** and **(C)**.

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. The Si Darlington transistor pair of Fig. 1 has negligible leakage current, and $\beta_1 = \beta_2 = 50$. Let $V_{CC} = 12V$; $R_E = 1\ k\Omega$, and $R2 \rightarrow \infty$. (i) Find the value of R_1 needed to bias the circuit so that $V_{CEQ2} = 6V$. (ii) With R_1 as found in part a, find V_{CEQ1}. **(8)**
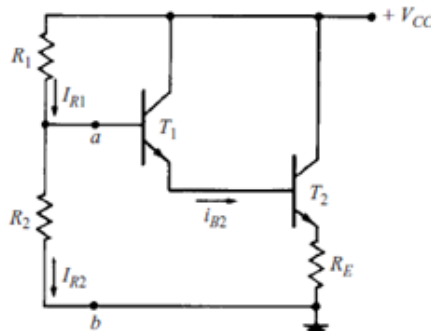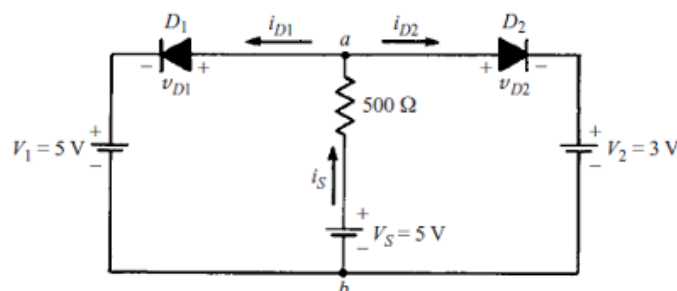

Fig. 1

b. What is load line? Discuss why ac load line differs from the dc load line. Draw the ac load line for a CE configuration amplifier and find the Q-point. **(8)**

Q.3 a. In the circuit of Fig. 2, Diodes $D1$ and $D2$ are ideal diodes. Find I_{D1} and I_{D2}. **(8)**

b. A Zener diode has the specifications $V_Z = 5.2$ V and $P_{Dmax} = 260$ mW. Assume $R_{Z=0}$ (i) Find the maximum allowable current i_Z when the Zener diode is acting as a regulator. (ii) If a single-loop circuit consists of an ideal 15-V dc source V_S, a variable resistor R, and the described Zener diode, find the range of values of R for which the Zener diode remain in constant reverse breakdown with no danger of failure. **(8)**

Q.4   a   Describe the construction and operation of JFET's. Explain the parameters g_m, I_{DSS}, I_{GSS}, $V_{GS(OFF)}$ and V_P. Describe the transconductance curve for a JFET and explain how it relates to the drain characteristic curve. **(8)**

b. Explain the operation of a class B push pull power amplifier with a neat circuit diagram and waveforms. Determine its collector efficiency. What is cross over distortion and how do you eliminate it in the above power amplifier? **(8)**

Q.5   a.   An amplifier has a voltage gain of 4000. It's input impedance is 2 K ohm and output impedance is 60 K ohm. Calculate the voltage gain, input and output impedance of the circuit if 5% of the feedback is fed in the form of series negative voltage feedback. **(8)**

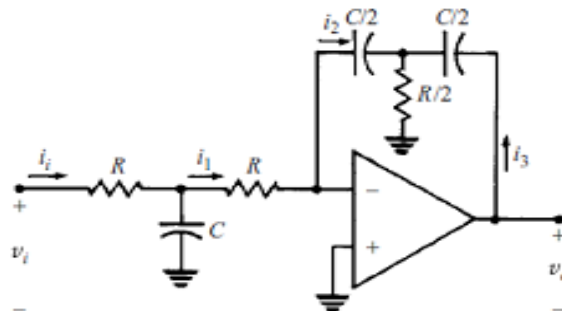b. Find the relationship between v_o and v_i in the circuit of Fig. 3. **(8)**

Fig. 3

Q.6   a.   The time constant of the differentiator circuit of Fig.4 is $\tau = 1$ms, and $v_c(0^-) = 0$

     (i)   Find the value of the feedback resistor R_f.
     (ii)   Derive the transfer function.
     (iii)   Find the magnitude and phase at f= 1 kHz
     (iv)   If a resistor is added in series with the capacitor to limit the high frequency gain to 100, what should be the value of that resistor?

(10)
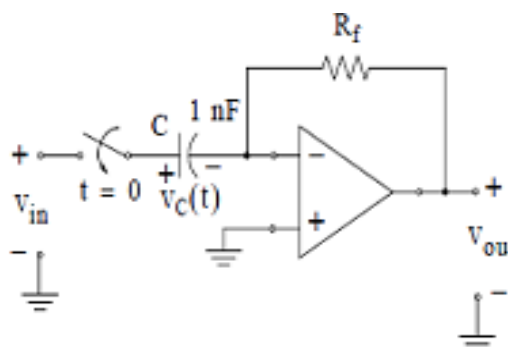
b. For the Schmitt trigger circuit of Fig. 5(a) below, the input signal v_s is as shown in Fig 5(b), find and sketch V_{+upper} and V_{+lower}.   **(6)**
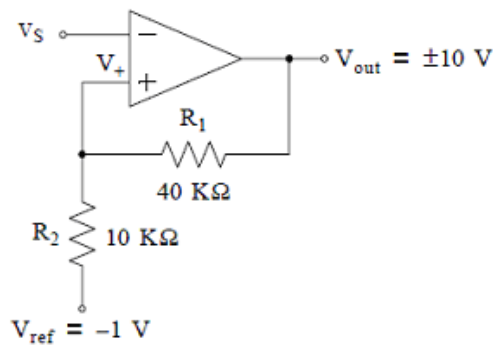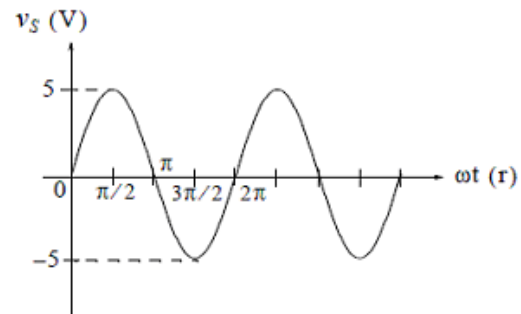

Fig. 5(a)

Fig. 5(b)

Q.7 a. Explain the use of an external pass transistor and current limiting in IC voltage regulator.   **(8)**

b. Implement the JK FF using NAND GATES ONLY.   **(8)**

Q.8 a. Prove that for a Wien Bridge oscillator the gain of amplifier should equal to δ i.e deviation where $\delta > 3$. Also derive expression for frequency of oscillation with suitable diagram   **(8)**

b. A combinational logic circuit is required which produces an output D from four input signals A, B, $C1$ and $C2$ according to the following rules.
  (i) If $C1$ and $C2$ are both 1, the output D must be 0.
  (ii) If $C1$ and $C2$ are both 0 the output D must be 1.
  (iii) If $C1=1$ and $C2=0$, then output D must be equal to input A.
  (iv) If $C1=0$ and $C2=1$, then output D must be equal to input B.

  (i)   Construct the truth table for D.
  (ii)   Construct the Karnaugh map for D.
  (iii) By combining 1s in the largest possible groups on the Karnaugh map, obtain an expression for D in the simplest sum-of-products form.
  (iv) Draw the gate implementation of the logic circuit to generate the output D using AND gate, OR gates and inverters.   **(8)**

Q.9   Write short note on any **TWO**:

  (i)   555 timer
  (ii) Transistor biasing techniques
  (iii) MOSFET.   **(2×8)**