Q.2 a. Explain with sketches n-well process of CMOS fabrication.

Ans: Figures of CMOS P-well process fig.1.9 (Page No: 16) except substrate is of p-type and well is of n-type.

Page No: 17 of Textbook

b. What is the advantages of E-beam masks? Explain the steps involved in making E-beam mask.

Ans: Page No: 26 of Textbook

Q.3 a. Derive an expression for Pull-up to Pull-down ratio for an n-MOS inverter driven through one or more pass transistors.

Ans: Page No:42-45 of Textbook

b. Write BiCMOS inverter circuit with MOS transistors for base current discharge and explain its operation.

Ans: BiCMOS inverter circuit with MOS transistors for base current discharge
Page No: 56 ,(figure 2.20) of Textbook

c. An inverter uses FETs with β_n=2.1mA/V^2 and β_p=1.8mA/V^2, the threshold voltages are given as V_{tn}=0.6V, V_{tp}=-0.7V and a supply voltage of V_{DD}=5V. Calculate midpoint voltage.

Ans:

$$V_m = \frac{V_{DD} - |V_{tp}| + \sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

Q4. a. Discuss λ -based C-MOS design rules for P-well and contacts.

Ans: Page No: 75 ,(figure 3.8) of Textbook
Page No: 80 (figure 3.11 bottom left fig. design rules only) of Textbook

b. Write the monochrome stick encoding of

i) 2-input CMOS NOR gate

Ans: Page No: 157 (figure 6.8C, only CMOS stick diagram) of Textbook

ii) Two-way selector with enable

Ans: Page No: 89 (figure 3.15, only stick diagram) of Textbook

Q.5 a. Obtain the expression for total delay for N stages of NMOS and CMOS inverters in terms of width factor 'e' and delay factor 'τ'.

Ans: Page No: 108 & 109 of Textbook

b. Define sheet resistance and standard unit of capacitance ΥC_g. Find the static and dynamic resistance of a minimum sized CMOS inverter.

Ans: Sheet resistance $(R_s)=\frac{\rho}{t}\Omega\Upsilon$

Standard unit of capacitance is gate to channel capacitance of a standard gate

Static on-state resistance of CMOS inverter is ∞, because for any static input one of MOS transistor of a CMOS inverter is off.

Dynamic resistance of a minimum sized CMOS inverter is 35kΩ

Page No: 98 (fig.4-3.b) of Textbook

Q.6 a. Write the scaling factors for the following device parameters

(i) Saturation current I_{dss}
(ii) Channel resistance R_{on}
(iii) Gate delay
(iv) Power speed product (P_T)

Ans: **Page No: 126, 127 & 128 of Textbook**

b. Explain the structured design of a parity generator with necessary blocks and write stick diagram of NMOS one bit parity generator cell.

Ans: **Page No: 166 & 167 of Textbook**

Q.7 a. What are the problems associated with the design of VLSI system. How to overcome these problems

Ans: Page No: 198 of Textbook

b. Draw and explain carry-select adder(6 bit) structure.

Ans: Page No: 209-210 of Textbook

c. Write Manchester carry-chain element and explain its operation.

Ans: Page No: 228 (figure 8.15) of Textbook

Q.8 a. Explain with circuit diagram
i) Six transistor static CMOS memory cell.
ii) CMOS pseudo-static D-flip flop

Ans:

i) Six transistor static CMOS memory cell
Circuit diagram **(Page No: 267, figure 9.7b of Textbook)**
Explanation **(Page No: 268 of Textbook1)**

ii) CMOS pseudo-static D-flipflop
Circuit diagram **(Page No: 273, figure 9.12 of Textbook)**

b. Explain the optimization of NMOS inverter.

Ans: Brief explanation **(Page No: 290 and 291 of Textbook).**

Q.9 Write short notes on

(i) System partitioning
Ans: Page no: 333 of Textbook

(ii) Design for testability
Ans: Page no: 334 &335 of Textbook

(iii) Testing combinational logic
Ans: Page no: 336 &337 of Textbook

(iv) Boundary Scan Test (BST)
Ans: Page no: 352 &353 of Textbook

Textbook

Basic VLSI Design By D A Pucknell, K Eshraghian Third Edition, PHI private Ltd. New delhi - 2001