

Time: 3 Hours

DECEMBER 2012

Max. Marks: 100

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. The performance equation of a CPU is $T = \frac{N \times S}{R}$, where T is the processor time to execute a program; while N, S and R are respectively _____, _____ and _____.

- (A) Number of instructions, Average number of steps and Number of Registers.
(B) Number of instructions, Average number of steps and Clock rate.
(C) Number of lines of a program, Size of program and Number of Registers.
(D) None of these

b. Return addresses in the case of subroutine nesting are used in

- (A) LIFO (B) FIFO
(C) LILO (D) FILO

c. Name the addressing mode in which the effective address is determined by the Index mode using the program counter in place of the general purpose register.

- (A) Indirect (B) Base-Indexed
(C) Relative (D) Auto-decrement

d. The full form of CPSR is

- (A) Current Program Special Register
(B) Control Program Status Register
(C) Current Program Status Register
(D) Conditional Program Special Register

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- e. _____ is an event that causes the execution of one program to be suspended and the execution of another program to begin.
- (A) Exception (B) Interrupt
(C) Subroutine (D) Tracker
- f. The approach in which “a special control unit may be provided to allow transfer of a block of data directly between an external device and the main memory, without continuous intervention by the processor” is called _____.
- (A) Direct Memory Access (B) Memory transfer
(C) Reading a memory (D) None of these
- g. Memories that consist of circuits capable of retaining their state as long as power is applied are known as _____.
- (A) Static memory (B) Power memory
(C) Dynamic memory (D) Circuit memory
- h. Techniques that automatically move program and data blocks into the physical main memory when they are required for execution are called _____.
- (A) Paging (B) Swapping
(C) Virtual Memory (D) Cache Memory
- i. In 4-bit CLA, the addition process requires only _____.
- (A) 4 gates (B) 1 XOR and 3 HA
(C) 2 gate delay (D) 5 FA
- j. The registers, the ALU, and the interconnecting bus are collectively referred to as the _____.
- (A) Datapath (B) Subpath
(C) Connecting path (D) None of these

Answer any FIVE Questions out of EIGHT Questions.**Each question carries 16 marks.**

- Q.2** a. With the help of diagram explain the different functional units of a Computer? (8)
- b. Represent (-23) in:
- (i) Sign-and-magnitude representation
(ii) 1's complement representation
(iii) 2's complement representation (4)
- c. Explain the use of following registers:
- (i) PC (ii) MAR
(iii) IR (iv) MDR (4)

- Q.3** a. Explain the process called subroutine nesting. (4)
- b. A two word instruction is stored in memory at an address designated by symbol W . The address field of the instruction (stored at $W + 1$) is designated by the symbol Y . The operand used during the execution of the instruction is stored at an address symbolized by Z . An index register contains the value X . State how Z is calculated from the other addresses if the addressing mode of the instruction is:
- | | | |
|----------------|---------------|-----|
| (i) Direct | (ii) Indirect | |
| (iii) Relative | (iv) Indexed | (8) |
- c. Write a program that can evaluate the expression
 $X = (A-B) * ((C - D * E) / F)$
in a single-accumulator processor, Assume that the processor has Load, Store, Multiply, Add instructions and that all values fit in the accumulator. (4)
- Q.4** a. What are the main advantages of using Input / Output interface? Why interfacing is used in digital computers? (8)
- b. Define Bus arbitration. Explain Centralized and Distributed arbitration process. (8)
- Q.5** a. Describe the Peripheral Component Interconnect (PCI) Bus Standards. (5)
- b. What are the sequences of events take place when the processor sends a command to the SCSI controller? (6)
- c. Explain how USB support Isochronous data. (5)
- Q.6** a. (i) How many 128×8 RAM chips are needed to provide a memory capacity of 2048 bytes?
(ii) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?
(iii) How many lines must be decoded for chip select? Specify the size of the decoder. (6)
- b. A digital computer has a memory unit of $64K \times 16$ and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.
(i) How many bits are there in the tag, index, block and words fields of the address format?
(ii) How many bits are there in each word of cache and how are they divided into functions? Include a valid bit.
(iii) How many blocks can the cache accommodate? (6)
- c. What do you mean by Memory – interleaving? (4)
- Q.7** a. Design a half adder as a 2 level AND OR circuit? Implement full adder circuit using 2 half adders. (6)

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- b. Explain the purpose of Disk controller.
- c. A certain magnetic disk has the following specification:
- Number of recording = 10
 - Number of tracks/surface = 256
 - Number of sectors/track = 32
 - Number of bytes/sector = 128
 - Disk rotation speed = 2400 rpm

Calculate the following:

- (i) Disk capacity
(ii) Transfer rate
(iii) Latency time

(6)

Q.8 a. Explain Restoring division and nonrestoring division process. Also, give algorithms for the two processes. **(8)**

b. Briefly discuss IEEE Standard Floating-point representation? Create the 32-bit single-precision IEEE standard representation of the decimal number – (0.625). **(4+4)**

Q.9 a. Write the actions required to execute the instructions Move(R1), R2. **(5)**

b. Distinguish between horizontal and vertical microinstruction. **(5)**

c. With the help of figure, explain multiple-bus organization. **(6)**