Subject: LOGIC DESIGN

Time: 3 Hours **JUNE 2011** **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. The BCD number for decimal 478 is

(A) 111011010 **(B)** 110001110011
(C) 010001111000 **(D)** 010011111000

b. Nibble is a group of

(A) 8 bits **(B)** 2 bits
(C) 3 bits **(D)** 4 bits

c. The output of a gate is high if all the inputs are high. Then it is a

(A) NAND **(B)** AND
(C) EX-OR **(D)** OR

d. How many flip-flops are required to implement a divide by 64?

(A) 64 **(B)** 32
(C) 16 **(D)** 6

e. Initially counter is reset to 0000, the terminal count of a modulus-13 binary counter is

(A) 0000 **(B)** 1011
(C) 1101 **(D)** 1100

f. The bit capacity of a memory that has 1024 addresses and can store 8 bits at each memory is

(A) 1024 **(B)** 8192
(C) 8 **(D)** 4096

g. A DRAM must be

(A) replaced periodically **(B)** refreshed periodically
(C) always enabled **(D)** programmed before each use

h. The 74LS83 is an example of a 4-bit parallel adder to expand this device to an 8 bit adder, you must

(A) Use four adders with no interconnections
(B) Use two adders and connect the sum outputs of one to the bit inputs of the other
(C) Use of eight adders
(D) Use two adders with the carry out of one connected to the carry input of the other

i. Sum of four bits can be performed by

(A) three EX-OR gates **(B)** three EX-NOR gates
(C) four EX-OR gates **(D)** none of them

j. Strobe signal is used in decoder to

(A) avoid more than one output active
(B) avoid more than one input active
(C) avoid glitches
(D) select the decoder

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Perform the following

(i) $(125)_{10} = (?)_2$ (ii) $(58.3)_{10} = (?)_8$
(iii) $(735)_8 = (?)_{16}$ (iv) $(A89C)_{16} = (?)_2$ **(8)**

b. What is alphanumeric code? Explain ASCII code. **(8)**

Q.3 a. Show that how NAND and NOR gates can be used as AND, OR and INVERT gates? **(8)**

b. Using K-map convert the following standard POS expression into a minimum SOP expression

$$(\overline{A}+\overline{B}+C+D)(A+\overline{B}+C+D)(A+B+C+\overline{D})(A+B+\overline{C}+D)(A+B+\overline{C}+\overline{D})$$

(8)

Q.4 a. Explain JK flip-flop with asynchronous inputs. Also explain propagation delay in a flip-flop with the help of waveforms. **(8)**

b. With neat diagram explain 4 bit parallel data transfer register using JK flip flop. **(8)**

Q.5 a. Express the decimal number –29 as a 6-bit number in the sign magnitude, 1's complement and 2's complement forms. **(4)**

b. Perform the following

(i) $(A29)_{16} + (8EC)_{16}$

(ii) Add the BCD numbers $(01001000) \& (00110100)$ **(4)**

c. Explain the feature of IC 74382 ALU. **(8)**

Q.6 a. Design a synchronous decade counter using JK flip flops. **(9)**

b. Design a ripple counter using DFF which will count up from 0101 to 1101. **(7)**

Q.7 a. Design a decimal to BCD code converter. **(8)**

b. Design and explain 8 bit comparator. **(8)**

Q.8 Design and explain with the help of waveform, a universal shift register. **(16)**

Q.9 a. Implement Full Adder using ROM. **(8)**

b. Explain the reading and writing operations in a DRAM cell. **(8)**