Diplete – ET (NEW SCHEME) – Code: DE56

Subject: ANALOG ELECTRONICS

Time: 3 Hours

JUNE 2011

56 Max. Marks: 100

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.

• Any required data not explicitly given, may be suitably assumed and stated.

Q.1 Choose the correct or the best alternative in the following:

 (2×10)

a. The CE amplifier circuits are preferred over CB amplifier circuits because they have

(A) lower amplification factor	(B) larger amplification factor
(C) high input and output resistance	(D) none of these

b. The input impedance of a JFET is _____ that of a ordinary transistor

(A) equal	(B) less than
(C) more than	(D) none of these

c. A maximum efficiency of class-B amplifier is

(A) 50 %	(B) 78.5 %
(C) 35 %	(D) 100 %

d. A non-inverting amplifier using op-amp employs the following type of feedback

(A) voltage-shunt	(B) current-shunt
(C) current-series	(D) voltage series

e. The max frequency $f_{max}\,$ at which we can obtain an undistorted output voltage of peak value $V_m\,$ is given by

(A) slew rate/ $6.28 \times V_{\rm m}$	(B) $6.28 \times V_{\rm m}$ /slew rate
(C) slew rate $\times 6.28$ / V _m	(D) slew rate $\times V_m/6.28$

f. The instrumentation amplifier has an important feature of

(A) high CMMR	(B) low CMMR
(C) low dc offset	(D) high dc offset

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g. LM 340 is a

(A) positive regulator (C) include both ranges (**B**) negative regulator (D) fixed regulator

StudentBounty.com h. If Differential gain A_d =3000 and Common Mode gain A_{cm} = 0.35 the CMMR is

(A) 1225	(B) 10000
(C) 80 dB	(D) Both (B) and (C)

i. The CMOS Schmitt Trigger offers the advantage of

(A) low input impedance and low power consumption (B) high input impedance and high power consumption (C) high input impedance and low power consumption (D) low input impedance and high power consumption

j. The IC fabrication consist of four distinct layers, the layer no.1 is

(A) thin n type material	(B) SiO $_2$ layer
(C) aluminium layer	(D) p type silicon substrate

Answer any FIVE Questions out of EIGHT Questions. Each question carries 16 marks.

Q.2	a.	List the basic processes used in the silicon planner technology, describe diffusion process in detail	the (8)
	b.	Compare the thin and thick film fabrication techniques	(8)
Q.3	a.	Draw an h parameter equivalent circuit for the CE unbypassed emitter configuration briefly explain the component of the model	bias (8)
	b.	Given $I_E = 2.5 \text{mA}$ $h_{fe} = 140$ $h_{oe} = 20 \mu S(\mu \text{mho})$ and $h_{ob} = 0.5 \mu S$. Determ the common emitter hybrid equivalent circuit.	nine (8)
Q.4	a.	Describe the following terms (i) Forward transfer admittance (ii) Output admittance (iii) Gate cutoff current (iv) Breakdown voltage	(8)
	b.	Determine the forward transfer admittance Y_{fs} of a FET, when the d current changes from 1mA to1.9 mA with a change in gate source vol-	rain tage

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from -3.3V to -3 V.

(8)

- Q.5 a. Draw the circuit diagram of class B transformer coupled output stage amplifier and explain its operation.
 - b. Describe the construction and working principle of liquid crystal cell.
- StudentBounty.com 0.6 a. Describe the characteristics of an ideal op-amp, how an ideal amplifier drives an infinite number of other devices.
 - b. For an inverting amplifier, find the voltage gain v_0/v_s using characteristics of an ideal op-omp i.e the open loop voltage gain AOL is negatively infinite (8)
- a. Find V_o for the adder-subtractor circuit shown in Fig.1 (8) **Q.7**



- b. Draw and describe the operation of practical AC voltage follower circuit. (8)
- **Q.8** a. Draw the circuit diagram of Phase shift oscillator and describe its operation.

(8)

b. For the monostable multivibrator circuit shown in Fig.2, $R = 100K\Omega$ and the time delay T = 100 ms. Calculate the value of C. (8)



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- StudentBounty.com Q.9 a. Describe the important performance parameters of series voltage regulator. List the value of each parameter as per data sheet of 7805.
 - b. Draw the functional diagram of the successive approximation ADC. Explain its operation.