**Code: DE09** **Subject: DIGITAL ELECTR**
**Time: 3 Hours** **Max. Marks:**

# JUNE 2011

**NOTE: There are 9 Questions in all.**

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

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**Q.1 Choose the correct or the best alternative in the following: (2×10)**

a. The parity of the binary number 11001110

**(A)** is even. **(B)** is not known
**(C)** is odd **(D)** is same as the number of zeros

b. The most suitable gate for comparing two bits is

**(A)** AND **(B)** OR
**(C)** NAND **(D)** EX-OR

c. The digital logic family has the maximum logic swing is

**(A)** $I^2L$ **(B)** ECL
**(C)** CMOS **(D)** TTL

d. The number of 4-line-to-16-line decoders required to make an 8-line-to-256-line Decoder is

**(A)** 16 **(B)** 17
**(C)** 32 **(D)** 64

e. A twisted-ring counter consisting of six FLIP-FLOPS will have

**(A)** 6 states **(B)** 12 states
**(C)** 64 states **(D)** 128 states

f. When representing in the following code the consecutive decimal numbers differ only in one bit is

**(A)** Excess-3 **(B)** Gray
**(C)** BCD **(D)** Hexadecimal

g. The speed of conversion is maximum in

**(A)** Successive-Approximation A/D converter
**(B)** Parallel-Comparator A/D converter
**(C)** Counter ramp A/D converter
**(D)** Dual-slope A/D converter

h. In an R-2R Ladder D/A converter, the input resistance is

**(A)** not same for all digital inputs **(B)** R for each input
**(C)** 2R for each input **(D)** 3R for each input

i. It is desired to have a 64X8 memory. The memories available are of 16X4 size. The number of memories required will be

**(A)** 8 **(B)** 6
**(C)** 4 **(D)** 2

j. The minimum number of bits required to represent negative numbers in the range of -1 to -9 using twos complement representation is

**(A)** 2 **(B)** 3
**(C)** 4 **(D)** 5

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**Answer any FIVE Questions out of EIGHT Questions.**
**Each question carries 16 marks.**

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**Q.2** a. Solve the equation $23.6_{10} = X_2$ for X **(6)**

b. Add -20 with +26 using 8 bit 2's complement arithmetic **(6)**

c. Convert the Decimal number 430 to its Excess-3 equivalent **(4)**

**Q.3** a. Show that $XY + \overline{XZ} + X\overline{Y}Z\ (XY + Z) = 1$ using Boolean Algebraic Theorems **(8)**

b. State and prove De-morgan's Theorems. **(8)**

**Q.4** a. What is a Tri-state Logic? Draw the logic diagram of Tri-state Logic Inverter and explain its operation with the help of truth table. **(8)**

b. Draw the K-map for the following function and reduce it.
$F(A, B, C, D) = \sum m(1,3,5,8,9,11,15) + d(2,13)$ **(8)**

**Q.5** a. What is full adder? Design the logic circuit for it using NAND gates only. **(10)**

b. Implement the following function using a 4 to 1 multiplexer
$F(A,B,C) = \sum m(1,3,5,6)$ **(6)**

**Q.6** a. What is an Encoder? Design a 10 line to 4 line Decimal to BCD encoder. **(8)**

b. Explain the operation of 4 bit digital comparator. **(8)**

**Q.7** a. Design a Mod-5 Synchronous counter. **(8)**

b. Give the circuit diagram of 4-bit SISO shift register and explain its working **(8)**

**Q.8** a. Differentiate between Static RAMs and Dynamic RAMs. Draw the logic diagram of a Static RAM cell and explain its operation. **(1**

b. Compare ROM, PROM, EPROM, UVEPROM, EEPROM. **(6)**

**Q.9** a. Explain the operation of Successive Approximation A/D Converter. List out its main Features. **(8)**

b. A 6 bit R-2R ladder D/A converter has a reference voltage of 6.5 V. It meets Standard linearity. Find

(i) The Resolution in Per cent
(ii) The Resolution in Volts
(iii) The Full Scale Voltage
(iv) The Output Voltage for the code 011100 **(8)**