Code: DC02 **Subject: FUNDAMENTALS OF ELECTRONI**
Time: 3 Hours **Max. Marks: 100**

JUNE 2011

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The input impedance of an ideal op-amp is_____

(A) Zero. **(B)** Infinity.
(C) 100Ω . **(D)** Less than one.

b. A resistor has a colour band sequence Green, Violet, Black and gold. Its value is_____

(A) 5.7 Ω ± 5%. **(B)** 57 Ω ± 5%.
(C) 570 Ω ± 5%. **(D)** 5.7 KΩ ± 5%.

c. Oscillators uses _____ feedback.

(A) Positive. **(B)** Negative.
(C) Both **(A)** and **(B).** **(D)** None of above.

d. An electron in the conduction band _____

(A) has no energy.
(B) has a less energy than an electron in the valance band.
(C) has equal energy than an electron in the valance band.
(D) has a higher energy than an electron in the valance band.

e. When the P-N junction is forward biased, width of depletion layer is _____

(A) reduced. **(B)** increased.
(C) same as unbiased. **(D)** none of above.

f. The Schottky barrier diode has _____

(A) one p-n junction. **(B)** two p-n junction.
(C) no p-n junction. **(D)** none of them is true.

g. In a junction transistor, which region is made narrower than the other tw regions _____

(A) collector region. **(B)** base region.
(C) emitter region. **(D)** none of above.

h. Which of the following is a universal gate _____

(A) AND **(B)** NAND
(C) OR **(D)** NOT

i. The main advantage of CMOS is _____

(A) high speed. **(B)** low noise margins.
(C) low power consumption. **(D)** none of above.

j The plastic DIP IC package is most widely used, because _____

(A) it has higher mechanical strength.
(B) it is only packing method available.
(C) other type of packing method is not reliable.
(D) it is much cheaper than other type of packages.

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain the working of electrolytic capacitor with the help of its constructional details. **(8)**

b. Explain how will you convert a current source into a voltage source. Also state and explain Thevenin's theorem. **(4+4)**

Q.3 a. What are intrinsic and extrinsic semiconductors? Explain effect of temperature on conductivity of semiconductor. **(4+4)**

b. What is p-n junction diode? How potential barrier is formed in a p-n junction diode? What is its significance? **(3+3+2)**

Q.4 a. Draw the V-I characteristics of Tunnel diode and explain its working principle. **(8)**

b. Explain the term doping and its need. Draw energy band diagram for N-type and P-type semiconductors and indicate the position of the Fermi, the donor and the acceptor levels. **(4+4)**

Q.5 a. Explain the transistor action with the help of suitable diagram and also explain need for transistor biasing. **(4+4)**

b. Compare the CB, CE and CC configurations of a transistor. Draw the input and output characteristics of a transistor in CB configuration. (

Q.6 a. Explain the differences between positive and negative feedback amplifier. What are advantages & disadvantages of negative feedback amplifier? **(4+4)**

b. With the help of a diagram, explain the working of FET as a switch. Also list out the applications of FET. **(4+4)**

Q.7 a. Prove the following using Boolean algebra

(i) $A\,(A+B) + A\,(B+C) + A\,(A+C) = A$

(ii) $(A+B)(\overline{A}+C)(B+C) = AC + B\overline{A}$ **(4+4)**

b. Minimize the following logic functions using K- Map

$$f(A, B, C, D) = \sum m(1,3,5,8,9,11,15) + d(2,13)$$ **(8)**

Q.8 a. Draw schematic diagram of TTL NAND gate and explain its working. **(8)**

b. Draw symbol of EX-OR gate and explain its working using truth table. Also realize EX-OR gate using four NAND gates only. **(4+4)**

Q.9 a. What is IC? Explain how a capacitor can be constructed in a monolithic IC. **(8)**

b. Draw the schematic diagram of Integrator and Voltage Follower using op-amp and explain its working. **(4+4)**