Subject: EMBEDDED SYSTEMS DESIGN

Time: 3 Hours **Max. Marks: 100**

JUNE 2011

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Identify which of these are real-time applications scenarios

(A) An on-line bus ticketing system
(B) Printing of annual report of a company's annual report
(C) Reconciling a day's transactions in an account book of a small company
(D) Examination system

b. Which of the following are commercially claimed RTOS

(A) Linux **(B)** Windows 7
(C) Windows 2000 **(D)** Vx works

c. With _____ the processor can read from or write to a port directly just as it would a register

(A) Port based I/O **(B)** Bus based I/O
(C) Memory mapped I/O **(D)** None of the above

d. Which of the following strategy is employed for overcoming the priority inversion problem?

(A) Abandon the notion of priorities altogether
(B) Have only two priority levels
(C) Allow for temporarily raising the priority of lower level priority process
(D) Use pre-emptive policies strictly based on priorities

e. A/an _____ routine must not call any RTOS function that might block the caller

(A) Timer **(B)** Serial Communication
(C) I/O **(D)** Interrupt

f. Where are the device drivers located in RTOS with a microkernel?

(A) In the kernel space
(B) In the user space
(C) In separately allocated space which is neither kernel space nor user space
(D) Anywhere in free space

g. For what types of operations is DMA useful?

(A) For large & fast data transfers between memory & I/O devices
(B) For large & slow data transfers between memory & I/O devices
(C) For slow & small data transfers between memory & I/O devices
(D) For small data transfers between memory & cache

h. When a process is rolled out of memory, it loses its ability to use the CPU (at least for a while). Describe another situation where a process loses its ability to use the CPU, but where the process does not get rolled out.

(A) When an interrupt occurs
(B) When thrashing occurs
(C) When deadlock occurs
(D) While swapping

i. Running, ready and block are concerned to

(A) Task State
(B) Semaphore State
(C) Mailbox State
(D) Pipe State

j. Semaphores and queues are _____ so that interface between modules is a function call

(A) Inherited
(B) Encapsulate
(C) Polymorphic
(D) Separate

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What is an embedded system? Give two examples for Small, Medium & sophisticated scale embedded systems. **(8)**

b. Explain top-down design process technology for Embedded System. **(4)**

c. Distinguish between a combinational circuit and a sequential circuit. **(4)**

Q.3 a. What is microcontroller? What are the functional circuits of a microcontroller and give advantages of writing embedded software in Assembly Language? **(6)**

b. What is GPP & ASIP? **(4)**

c. Explain the Hardware units of an Embedded System? Give advantag
writing embedded software in C Language. (

Q.4 a. Given a 120-step stepper motor with its own controller, write a C function *Rotate (int degrees)*, which, given the desired rotation amount in degrees (between 0 and 360), pulses a microcontroller's output port the correct number of times to achieve the desired rotation. **(6)**

b. Compute the memory needed in bytes to store a 4-bit digital encoding of a 3-second analog audio signal sampled every 10 milliseconds. **(4)**

c. Explain the synchronous, asynchronous and isosynchronous communication techniques. Give their respective applications. **(6)**

Q.5 a. Explain the following:- **(6)**
(i) PROM
(ii) Flash EEPROM
(iii) NVRAM

b. Explain ROM image, stack overhead and memory optimization. **(6)**

c. A given design with cache implemented has a main memory access cost of 20 cycles on a miss and two cycles on a hit. The same design without the cache has a main memory access cost of 16 cycles. Calculate the minimum hit rate of the cache to make the cache implementation worthwhile. **(4)**

Q.6 a. Define protocol. Name any two characteristics to be taken into account while interfacing a device. **(4)**

b. Define interrupt handler. Explain the difference between port-based I/O and bus-based I/O. **(4)**

c. Give advantages and disadvantages of using memory-mapped I/O versus standard I/O. **(4)**

d. Differentiate between parallel, serial and wireless communication. Give two common applications for each. **(4)**

Q.7 a. Differentiate between **(9)**

(i) Recursive and Reentrant function
(ii) Queue and Stack
(iii) RTOS and Non-RTOS

b. Define a semaphore and what is shared data problem? Briefly explain the problems that may arise while using semaphores? **(7)**

Q.8 a. Explain the following **(6)**
(i) Message Queue
(ii) Mailbox
(iii) Pipe

b. Explain any two features of RTOS. What are the strategies used by RTO interrupt source calls? (

c. What is memory management and how will it influence the real-time behaviour of an operating system? **(4)**

Q.9 a. Define the following:- **(6)**

(i) Inter process communication
(ii) Soft Real time systems
(iii) Hard Real time Systems

b. Differentiate between **(10)**
(i) Kernel space versus user space versus real-time space.
(ii) Monolithic kernel versus micro-kernel.