AMIETE – ET (OLD SCHEME)

Code: AE27 **Subject: DIGITAL HARDWARE DESIGN**
Time: 3 Hours **Max. Marks: 100**

JUNE 2011

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Horizontal and vertical formats are used in

(A) Register file **(B)** ALU
(C) Counters **(D)** Microprogram controller

b. Product of sums is a Boolean expression containing -------- terms.

(A) OR **(B)** AND
(C) NOR **(D)** NAND

c. A system in which signals have values from a continuous set is

(A) Mixed **(B)** Digital
(C) Analog **(D)** All of above

d. When two or more binary state variables change value in response to a change in an input variable is said to be ---------- condition and occurs in ---------- sequential circuit.

(A) Race, synchronous **(B)** Race, asynchronous
(C) Critical, asynchronous **(D)** Critical, synchronous

e. Process statement in VHDL implements the following model

(A) Data flow model **(B)** Structural model
(C) Both (A) and (B) **(D)** Behavioral model

f. Programmable Array Logic (PAL) has ---------- AND array and ---------- OR array

(A) Programmable, fixed **(B)** Fixed, Programmable
(C) Programmable, programmable **(D)** Fixed, fixed

g. Storage modules and functional modules belong to

(A) Bus subsystem **(B)** Control subsystem
(C) Both **(A)** and **(B)** **(D)** Data Subsystem

h. 4-to-16 decoder is designed using ---------- 2-to-4 decoders with enable

(A) 3 **(B)** 5
(C) 6 **(D)** 4

i. The following implements the function of AND-OR-INVERT

(A) AND-NOR, NAND-XNOR **(B)** AND-NOR, NAND-NOR
(C) AND-NOR, NAND-AND **(D)** AND-NOR, NAND-NAND

j. Basic operations of flip-flop are mentioned in the following table

(A) State table **(B)** Characteristic table
(C) Excitation table **(D)** Implication table

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Compare analog and digital signals. **(3)**

b. Explain the following levels of implementation for a digital design: **(6)**
(i) Modular
(ii) Logical
(iii) Physical

c. Explain various computer aided design tools purposes. **(7)**

Q.3 a. Convert the following expression into sum of products and product of sums:
x' + x(x + y')(y + z') **(4)**

b. Simplify the following Boolean expressions, using three-variable Karnaugh's map. Simplify the following Boolean expressions, using three-variable Karnaugh's map. **(6)**
(i) xy+ x′y′z′ + x′yz′
(ii) A′B + BC′ + B′C′

c. Explain how functional decomposition is used in combinational circuits. Give an example. **(6)**

Q.4 a. Implement four variable decomposition chart for
$f(w,x,y,z)=\sum(1,3,6,10,13,15)$ **(10)**

b. Mention various components of the following: **(6)**
(i) Data subsystem
(ii) Control subsystem

Q.5 a. Explain binary encoder and binary decoder and give an example for illustration. **(6)**

b. Design 16×1 multiplexer using 8×1 and 2×1 multiplexer. **(4)**

c. Design 4-bit bi-directional shift register and explain its functionality. **(6)**

Q.6 a. Compare and contrast the following modes used in VHDL: **(6)**
(i) Behavioral Model
(ii) Data Flow Model
(iii) Structural Model

b. Draw the 4×4 ROM MOS-implementation structure and explain different types of ROM modules? **(10)**

Q.7 a. Explain synchronous and asynchronous sequential machine. Give an example for each. **(5)**

b. Reduce the number of states in the following state table and tabulate the reduced state table: **(5)**

Present State	Next State		Output	
	x =0	*x=1*	*x=0*	*x=1*
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

c. For the bit pattern, 1100 design Mealy machine and Moore machine. **(6)**

Q.8 a. Write a VHDL-program to implement full-adder using structural style-modelling. Draw the timing wave-form of its simulation results by considering any four cases. **(8)**

b. Draw ASM chart of a serial adder and synthesize the logic circuit. **(8)**

Q.9 a. An asynchronous sequential circuit is described by the excitation and output functions: **(8)**

$$m = x_1 x_2' + (x_1 + x_2') y$$
$$z = y$$

Answer the following:
(i) Draw the logic diagram of the circuit
(ii) Derive transition table and output map
(iii) Obtain two-state flow table
(iv) Describe in words the behavior of the circuit.

b. Explain the operation of microinstruction sequencing. Explain various cycles in microinstruction. **(4)**

c. Explain state assignment technique. **(4)**