Subject: COMPUTER ORGANIZATION

Time: 3 Hours **Max. Marks: 100**

JUNE 2011

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The average time required to reach a storage location in memory and obtain its contents is called the

(A) Seek time **(B)** Turnaround time
(C) Access time **(D)** Transfer time

b. Translation from symbolic program into Binary is done in

(A) Two passes **(B)** Directly
(C) Three passes **(D)** Four passes

c. ASCII code for Line feed character is

(A) 0C **(B)** 0D
(C) 0A **(D)** none

d. A _____ is a hardware device that intervenes when two potential bus masters want control of the bus at the same time.

(A) System Bus **(B)** Bus Arbitration Unit
(C) Cache Controller **(D)** Peripheral Processing Unit

e. Arithmetic shift left operation

(A) produces the same result as obtained with logical shift left operation.
(B) causes the sign bit to remain always unchanged.
(C) needs additional hardware to preserve the sign bit.
(D) is not applicable for signed 2's complement representation.

f. When the I/O devices and the memory share the same address space the arrangement is called

(A) Memory Mapped I/O **(B)** I/O Mapped I/O
(C) Standard I/O **(D)** None

g. In a vectored interrupt

(A) the branch address is assigned to a fixed location in memory
(B) the interrupting source supplies the branch information to the processor through an interrupt vector
(C) the branch address is obtained from a register in the processor
(D) none of the above

h. When the processor constantly checks the status of an I/O device, this is called:

(A) Memory Mapped I/O. **(B)** Asynchronous communication.
(C) Synchronous communication. **(D)** Polling

i. Which of the following statements on DRAM are correct?
(i) Page mode read operation is faster than RAS read.
(ii) RAS input remains active during column address strobe.
(iii) The row and column addresses are strobed into the internal buffers using RAS and CAS inputs respectively.

(A) (i) & (iii) **(B)** (i) & (ii)
(C) All **(D)** (iii)

j. Which of the following memories must be refreshed many times per second?

(A) Static RAM **(B)** Dynamic ROM
(C) EPROM **(D)** None.

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. How does the computer manage overflow? Explain with an example. **(6)**

b. Explain the use of following registers MAR, MBR, PC and IR. **(4)**

c. Explain the developments made during different generations of computers. **(6)**

Q.3 a. Explain the program for evaluation of F = A*B+C*D/E using zero address instructions. **(4)**

b. What are the steps required for execution of an instruction? How these ... performed by the CPU?

c. Write short notes on:
(i) Immediate addressing
(ii) Direct addressing
(iii) Indirect addressing. **(6)**

Q.4 a. Describe the three types of Input / Output techniques, viz., Programmed Input / Output Interrupt driven Input / Output and Direct Memory Access? **(12)**

b. Differentiate between a subroutine and an interrupt-service routine? **(4)**

Q.5 a. Write short notes on USB and PCI bus. **(10)**

b. Write short note on interface circuits. **(6)**

Q.6 a. What are the commonly used terms for identifying comparative behaviour of various memory devices and technologies? **(10)**

b. Describe the importance of cache memory and explain set associative mapping with a neat diagram. **(6)**

Q.7 a. Add the numbers 65 and 75 in 8 bit register in signed 2's complement notation. **(6)**

b. Explain the design of fast adder with suitable diagram. **(10)**

Q.8 a. Explain about IEEE standard representation of floating point numbers. **(10)**

b. Explain the floating point Addition – subtraction unit with neat diagram. **(6)**

Q.9 a. Write the sequence of control steps required for single bus organisation for the instruction:
Add the contents of memory location NUM to register R1.
Assume that each instruction consists of two words. The first word specifies the operation and the addressing mode, the second word contains the number NUM. **(10)**

b. Write short notes on Hardwired Control Unit. **(6)**