

AMIETE –CS/IT (OLD SCHEME)

Code: AC03 / AT03

Time: 3 Hours

JUNE 2011

Subject: BASIC ELECTRONICS &
DIGITAL CIRCUITS

Max. Marks: 100

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1 Choose the correct or the best alternative in the following: (2×10)

- a. Avalanche multiplication is caused by
- (A) Disruption of covalent bond by collision
(B) Discrete rupture of bonds
(C) (A) and (B) both
(D) None of these
- b. In an emitter follower with $R_L = 10\text{ K}$, given $h_{fe} = 99$, $h_{oe} = \frac{1}{40} \times 10^{-3}$, $h_{ie} = 1\text{ K}$, the value of current gain and input impedance are given by
- (A) 25 and 250 K (B) 80 and 800 K
(C) 99 and 990 K (D) 100 and 1000 K
- c. The low frequency response of an RC coupled circuit can be improved by
- (A) Increasing load resistance (B) Decreasing load resistance
(C) Increasing coupling capacitor (D) Decreasing coupling capacitor
- d. In a JFET, if the gate voltage V_{gs} is made more negative, then
- (A) Channel conductivity increases (B) Depletion region decreases
(C) Channel conductivity decreases (D) Channel current increases
- e. Oscillators have
- (A) No feedback (B) Negative feedback
(C) Positive feedback (D) Either positive or negative feedback
- f. The output of an op-amp increases 5 V in 12 μs . The slew rate is
- (A) 96 V/ μs (B) 0.67 V/ μs
(C) 1.5 V/ μs (D) None of the above

- g. The 2's complement representations of the decimal number -4 is
- (A) 0100 (B) 1100
(C) 1011 (D) 1010
- h. A binary to decimal decoder is called 1 to 10 decimal because
- (A) At a time one input is high
(B) Output is high only if all inputs are high
(C) Only one of its output lines is high at a time
(D) It has 10 input lines
- i. In JK flip-flop if $K = \bar{J}$, the resulting flip-flop is
- (A) SR flip-flop (B) JK Flip-flop
(C) D flip-flop (D) T flip-flop
- j. A shift register is a cascade of
- (A) D type flip-flop (B) T type latch
(C) SR flip-flops (D) None of these

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain the following terms: (i) Avalanche breakdown (ii) Zener breakdown (iii) Knee voltage (8)

b. Explain how a BJT can be used as a switch (8)

Q.3 a. Given $h_{ie} = 1K\Omega$, $h_{fe} = 100$, draw the h-parameter equivalent circuit of the amplifier shown in Fig.1. Calculate the input impedance, output impedance, current gain and voltage gain using this equivalent circuit. (10)

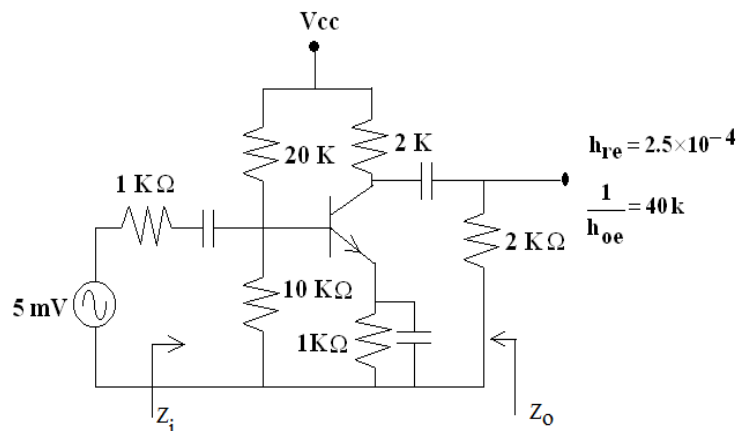


Fig. 1

- b. Draw the circuit of a cascode amplifier and explain its operation and its use. (6)
- Q.4** a. Draw the logic symbols and explain the operation of a D type and a T type flip-flop. (6)
- b. Explain the operation of 4 stage ring counter using JK flip-flops. (8)
- c. What is the difference between synchronous and asynchronous counter? (2)
- Q.5** a. Explain the basic ECL logic OR/NOR gate with a suitable diagram. (10)
- b. Differentiate between saturated and nonsaturated logic and also explain what is tristate logic. (6)
- Q.6** a. For circuit shown in Fig.2, determine I_D , V_{GS} and V_{DS} for $|I_{DSS}| = 4 \text{ mA}$, $V_p = 4 \text{ V}$ (8)

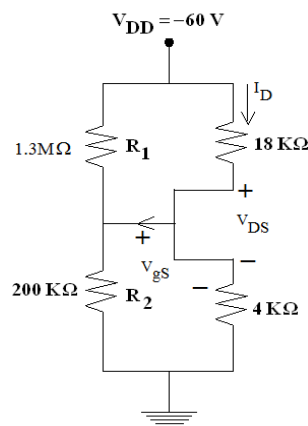


Fig. 2

- b. Draw the circuit diagram of Colpitt's oscillator and explain its working. (8)
- Q.7** a. The two input terminals of an op-amp are connected to voltage signals of strength $745 \mu\text{V}$ and $740 \mu\text{V}$ respectively. The gain of the op-amp in differential mode is 5×10^5 and its CMRR is 80 dB. Calculate the output voltage and percentage error due to common mode. (8)
- b. Realise a circuit to obtain $V_{\text{out}} = -2V_1 + 3V_2 + 4V_3$ using an op-amp. Use minimum value of resistance as $10 \text{ K}\Omega$. (8)
- Q.8** a. A half wave rectifier uses a diode with a forward resistance of 100Ω . If the input ac voltage is 220 V(rms) and the load resistance is of $2 \text{ K}\Omega$. Determine (i) I_{max} , I_{dc} and I_{rms} (ii) peak inverse voltage when the diode is ideal (iii) load output voltage (iv) dc output power and ac input power (v) ripple factor (vi) transformer utilization factor (vii) rectification efficiency. (10)
- b. Obtain the simplified expression in SOP form for the following Boolean function using K map. $Z = \overline{A} \overline{B} \overline{C} \overline{D} + \overline{A} \overline{B} C \overline{D} + A \overline{B} \overline{C} \overline{D} + \overline{A} C \overline{D} + A \overline{B} C \overline{D}$ (6)

Q.9 Write short notes on any **TWO** of the following:

- (i) Parity check generator
- (ii) CMOS as inverter
- (iii) PLA and PAL
- (iv) EPROM and EEPROM.

(8×2)