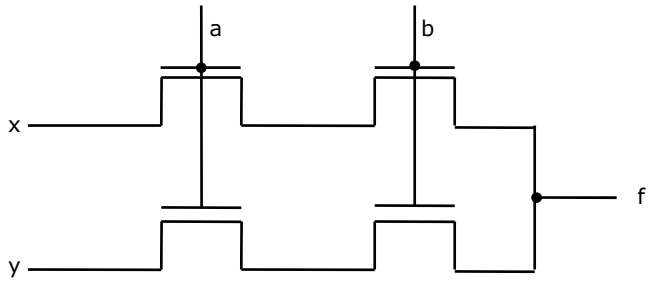
SECTION - A

1. Fill in the blanks:

(i) For the digital in figure, the expression for the output f is _____



(ii) In interleaved memory organization, consecutive words are stored in consecutive memory modules in _____ interleaving, whereas consecutive words are stored within the module in _____ interleaving.

(iii) Consider the number given by the decimal expression:

$16^3 * 9 + 16^2 * 7 + 16 * 5 + 3$

The number of 1's in the unsigned binary representation of the number is _____.

(iv) Using the 8087 arithmetic coprocessor with the 8087 CPU requires that the 8087 CPU is operated _____.

(v) When two 4-bit binary number $A = a_3a_2a_1a_0$ and $B = b_3b_2b_1b_0$ are multiplied, the digit c_1 of the product C is given by _____

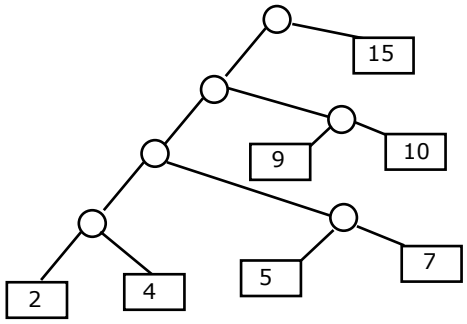
(vi) Consider the following PASCAL program segment:

```
if i mode 2 = 0 then
        while i > = 0 do
          begin
            i:=i div 2;
            if i mod 2 < > 0 do then i:=i – 1
                else i:=i – 2
end
```

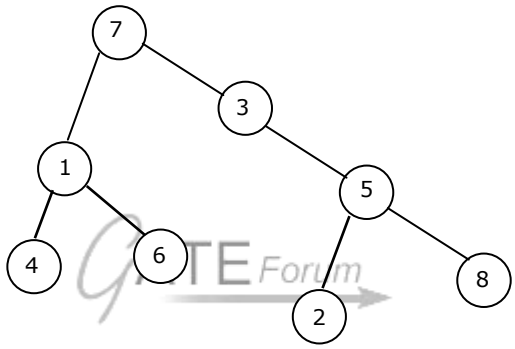
An appropriate loop-invariant for the while-loop is _____

(vii) The minimum number of comparisons required to sort 5 elements is _____

(viii) The weighted external path length of the binary tree in figure is _____



(ix) If the binary tree in figure is traversed in inorder, then the order in which the nodes will be visited is _____



(x) Consider the following recursive definition of fib:

fib (n) : = if n = 0 then 1

else if n = 1 than 1

else fib (n – 1) + fib (n – 2)

The number of times fib is called (including the first call) for an evaluation of fib (7) is _____

(xi) The arithmetic expression : $(a+b)*c-d/e**f$ is to be evaluated on a two-address machine, where each operands, the number of registers required to evaluate this expression is _____. The number of memory access of operand is _____.

(xii) A given set of processes can be implemented by using only **parbegin/parend** statement, if the precedence graph of these processes is _____

(xiii) The number of integer-triples (i.j.k) with $1 \le i.j.k \le 300$ such that i + j + k is divisible by 3 is _____

(xiv) If the longest chain in a partial order is of length n then the partial order can be written as a _____ of n antichains.

(xv) The maximum number of possible edges in an undirected graph with a vertices and k components is _____.

2. Match the pairs in the following questions by writing the corresponding le... only.

(i)

(A) IEEE 488	(P) specifies the interface for connecting a single device
(B) IEEE 796	(Q) specifies the bus standard for connecting a computer to other devices including CPU's
(C) IEEE 696	(R) specifies the standard for an instrumentation bus
(D) RS232-C	(S) specifies the bus standard for the "backplane" bus called multibus.

(ii) For the 8086 microprocessor:

(A) RQ/GT	(P) Used by processor for holding the bus for consecutive instruction cycles.
(B) LOCK	(Q) Used for extending the memory or I/O cycle times
(C) HOLD	(R) Used for getting hold of processor bus in minimum bus mode
(D) READY	(S) Used for requesting processor bus in minimum bus mode.

(iii)

(A) Buddy system	(P) Run-time type specification
(B) Interpretation	(Q) Segmentation
(C) Pointer type	(R) Memory allocation
(D) Virtual memory	(S) Garbage collection

(iv)

(A) The number distinct binary trees with n nodes	(P) $\frac{n!}{2}$
(B) The number of binary strings of length of 2n with an equal number of 0's and 1's	(Q) $\binom{3n}{n}$
(C) The number of even permutations of n objects	(R) $\binom{2n}{n}$
(D) The number of binary strings of length 6m which are palindromes with 2n 0's.	(S) $\frac{1}{n+1}\binom{2n}{n}$

3. Choose the correct alternatives (more than one may be correct) and writ... corresponding letters only:

(i) The advantages of CMOS technology over a MOS is:

(a) lower power dissipation

(b) greater speed

(c) smaller chip size

(d) fewer masks for fabrication

(e) none of the above

(ii) Advantage of synchronous sequential circuits over asynchronous ones is:

(a) faster operation

(b) ease of avoiding problems due to hazards

(c) lower hardware requirement

(d) better noise immunity

(e) none of the above

(iii) The total size of address space is a virtual memory systems is limited by

(a) the length of MAR

(b) the available secondary storage

(c) the available main memory

(d) all of the above

(e) none of the above

(iv) The TRAP interrupt mechanism of the 8085 microprocessor:

(a) executes an instruction supplied by an external device through the INTA signal

(b) executes an instruction from memory location 20H

(c) executes a NOP

(d) none of the above

(v) The ALE line of an 8085 microprocessor is used to:

(a) latch the output of an I/O instruction into an external latch

(b) deactivate the chip-select signal from memory devices

(c) latch the 8 bits of address lines AD7-AD0 into an external latch

(d) find the interrupt enable status of the TRAP interrupt

(e) None of the above

(vi) Kruskal's algorithm for finding a minimum spanning tree of a weighted g... G with vertices and m edges has the time complexity of:

(a) $O(n^2)$

(b) $O(mn)$

(c) $O(m+n)$

(d) $O(m \log n)$

(e) $O(m^2)$

(vii) The following sequence of operations is performed on a stack:

PUSH (10), PUSH (20), POP, PUSH (10), PUSH (20), POP, POP, POP, PUSH (20), POP

The sequence of values popped out is:

(a) 20, 10, 20, 10, 20

(b) 20, 20, 10, 10, 20

(c) 10, 20, 20, 10, 20

(d) 20, 20, 10, 20, 10

(viii) Consider the following Pascal function:

```
function X (M:integer) : integer;
var i:integer;
begin
   i = 0;
   while i*i<M do i; =i+1
   X;=i
end
```

The function call X(N), if N is positive, will return

(a) $\left(\sqrt{N}\right)$

(b) $\left(\sqrt{N}\right)+1$

(c) $\left[\sqrt{N}\right]$

(d) $\left[\sqrt{N}\right]+1$

(e) None of the above

(ix) A "link editor" is a program that:

(a) matches the parameters of the macro-definition with locations of the parameters of the macro call

(b) matches external names of one program with their location in programs

(c) matches the parameters of subroutine definition with the location of parameters of subroutine call.

(d) acts as link between text editor and the user

(e) acts as a link between compiler and user program.

(x) Indicate all the true statements from the following:

(a) Recursive descent parsing cannot be used for grammar with left recursion.

(b) The intermediate form the representing expressions which is best suited for code optimization is the post fix form.

(c) A programming language not supporting either recursion or pointer type does not need the support of dynamic memory allocation.

(d) Although C does not support call by name parameter passing, the effect can be correctly simulated in C.

(e) No feature of Pascal violates strong typing in Pascal.

(xi) Indicate all the false statements from the statements given below:

(a) The amount of virtual memory available is limited by the availability of secondary storage.

(b) Any implementation of a critical section requires the use of an indivisible machine-instruction, such as test-and-set.

(c) The LRU page replacement policy may cause hashing for some type of programs.

(d) The best fit techniques for memory allocation ensures the memory will never be fragmented.

(xii) If F_1, F_2 and F_3 are propositional formulae such that $F_1 \wedge F_2 \rightarrow F_3$ and $F_1 \wedge F_1 \rightarrow \sim F_2$ are both tautologies, then which of the following is true:

(a) Both F_1 and F_2 are tautologies

(b) The conjunction $F_1 \wedge F_2$ is not satisfiable

(c) Neither is tautologous

(d) Neither is satisfiable

(e) None of the above

(xiii) Let $r = 1(1+0)^*, s = 11^*0$ and $t = 1^*0$ be three regular expressions. Which one of the following is true?

(a) $L(s) \subseteq L(r)$ and $L(s) \subseteq L(t)$

(b) $L(r) \subseteq L(s)$ and $L(s) \subseteq L(t)$

(c) $L(s) \subseteq L(t)$ and $L(s) \subseteq L(r)$

(d) $L(t) \subseteq L(s)$ and $L(s) \subseteq L(r)$

(e) None of the above

(xiv) Which one of the following is the strongest correct statement about a finite language over some finite alphabet $\sum$?

(a) It could be undecidable

(b) It is Turing-machine recognizable

(c) It is a context-sensitive language

(d) It is a regular language

(e) None of the above

4. Give short answers to the following questions:

(i) Convert the following Pascal statement to a single assignment statement:

if x > 5 they y:=true

else y:=false;

(ii) Convert the Pascal statement *repeat S until* B; into an equivalent Pascal statement that uses the *while* construct.

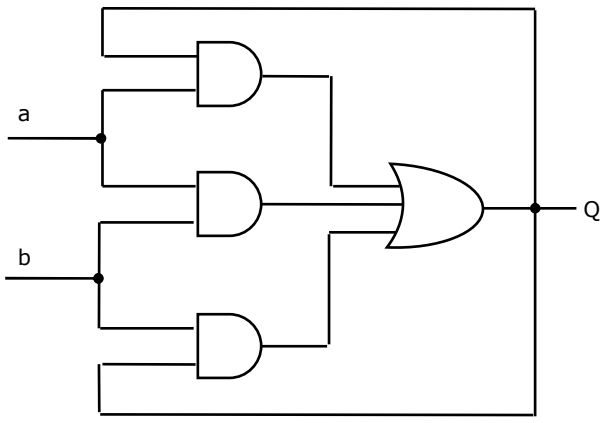
(iii) Obtain the optimal binary search tree with equal probabilities for the identifier set $(a_1, a_2, a_3) = (\text{if, stop,while})$

(iv) If a finite axiom system A for a theory is complete and consistent, then is every subsystem of A complete and consistent? Explain briefly.

SECTION – B

5. (a) Analyse the circuit in figure and complete the following table:

a	b	Q_n
0	0	
0	1	
1	0	
1	1	

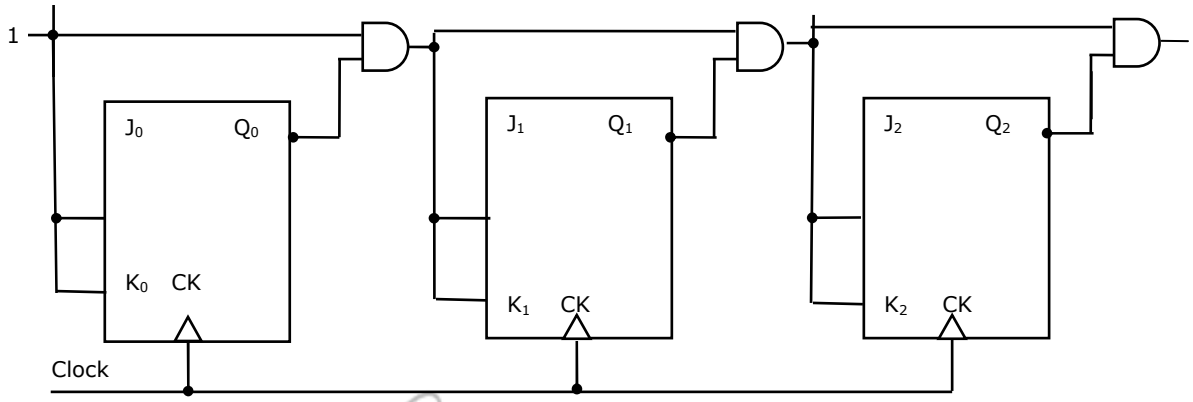


(b) Find the minimum sum of products form of the logic function.

$f(A,B,C,D) = \sum m(0,2,8,10,15) + \sum d(3,11,12,14)$

Where m and d denote the min-terms and don't cares respectively.

(c) Find the maximum clock frequency at which the counter in figure, can be operated. Assume that the propagation delay through each flip-flop and AND gate is 10 ns. Also assume that the setup time for the JK inputs of the flip-flops is negligible.



6. (a) Using D flip-flop and gates, design a parallel-in/serial-out shift register that shifts data from left to right with the following input lines:

(i) Clock CLK

(ii) Three parallel data inputs A, B, c

(iii) Serial input S

(iv) Control input load / $\overline{\text{SHIFT}}$.

(b) Design a 1024 bit serial-in/serial-out unidirectional shift register using a 1K $\times$ 1 bit RAM with data input D_{in}, data output D_{out} and control input READ/$\overline{\text{WRITE}}$. You may assume that availability of standard SSI and MSI components such as gates, registers and counters.

7. It is required to design a hardwired controller to handle the fetch cycle of a single address of an indexed instruction should be derived in the fetch cycle itself. Assume that the lower order 8 bits of an instruction constitute the operand field.

(a) Give the register transfer sequence for realizing the above instruction fetch cycle.

(b) Draw the logic schematic of the hardwired controller including the date path.

8. (a) Consider an 8085 based system operating with the following specification:

Crystal frequency : 6 MHz

ROM map : 0000 through 07FF

RAM map : 1000 through 17 FF:

ROM requires one wait state.

RAM requires no wait state.

Determine the instruction cycle time for each of the following instructions:

(i) ORI A, 22

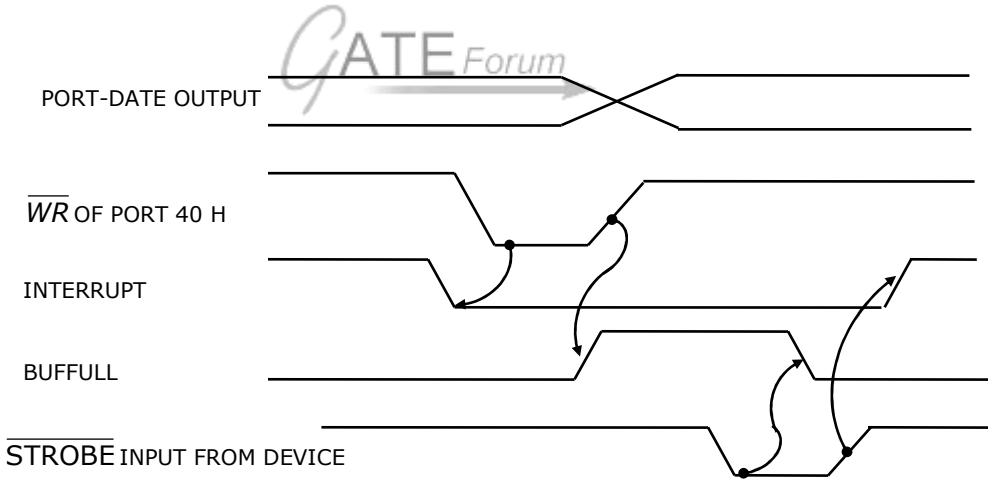
(ii) DCR M

Assume the following initial conditions of the CPU registers (in hex) for each of the instructions:

A = 55, B = AA, C = F7, D = 10, H = 10, L = FF, PC = 0200, SP = 17FO.

(b) Developing an output port interface (draw a block schematic) for an 8085 based system with a demultiplexed address bus which incorporates a handshake protocol as per the timing diagram given in figure. The interface should include a status input port at I/O address 40H which reads the INTERRUPT and BUFFFULL signals through the most significant bit and the least significant bit, respectively. The output data port is at the same I/O address 40H and is activated by a write operation. Assume the availability of SSI and MSI level components only.

Write a short program segment which performs a 200 H byte programmed I/O data transfer to the device from memory address 3400 H,



9. (a) Consider the following pseudo-code
(all data items are of type integer):

```
Procedure P (a, b, c);
            a:=2;
            c:=a+b;
end {P}
begin
            x:=1
            y:=5;
```

```
        z:=100;
        P(x,x*y,z);
        Write ('x=',x,z=',z)
    end:
```

Determine its output, if the parameters are passed to the procedure P by (i) value, (ii) reference and (iii) name.

(b) For the following pseudo-code, indicate the output, if

(i) static scope rules and (ii) dynamic scope rules are used

```
Var, a, b : inteer;
Procedure P;
    a:=5; b:=10
 end {P};
procedure Q;
var a, b : integer;
P;
end {Q};
begin
a:=1; b:=2;
Q;
Write ('a =', a, 'b=',b)
end.
```


10. Consider the following grammar for arithmetic expression using binary operators – and/which are not associative:

$$E \rightarrow E - T \mid T$$

$$T \rightarrow \frac{T}{F \mid F}$$

$$F \rightarrow (E)\, id$$

(E is the start symbol)

(a) Is this grammar unambiguous? If so, what is the relative precedence between – and/if not, give an unambiguous grammar that gives/precedence over -

(b) Does the grammar allow expressions with redundant parentheses as in (id/id) or in id-(id/id)? If so, convert the grammar into one which does not generate expressions with redundant parentheses. Do this with minimum number of changes to the given production rules and adding at most one more production rule.

11. Consider the following scheme for implementing a critical section in a situ... with three processes P_j and P_k.

```
Pi;
repeat
        flag [i]:=true;
while flag [j] or flag [k] do
        case turn of
        j : if flag [j] then
        begin
        flag [i]:=false;
        while turn ≠ i do skip;
        flag [i] : true
        end;
k : if flag [k] then
        begin
        flag [i]:=false,
        while turn ≠ i do skip;
        flag [i]:=true
        end
end
critical section
if turn = i then turn:=j;
flag [i]:=false
non-critical section
until false;
```


(a) Does the scheme ensure mutual exclusion in the critical section? Briefly explain.

(b) Is there a situation in which a waiting process can never enter the critical section? If so, explain and suggest modifications to the code to solve this problem.

12. Suppose, a database consists of the following relations:

SUPPLIER (SCODE, SNAME, CITY)

PART (PCODE, PNAME, PDESC, CITY)

PROJECTS (PRCODE, PRNAME, CITY)

SPRR (SCODE, PCODE, PRCODE, QJY)

(a) Write SQL programs corresponding to the following queries:

(i) Print PCODE value for parts supplied to any project in DELHI by a suppli... in DELHI.

(ii) Print all triples (CITY, PCODE, CITY), such that a supplier in the first city supplies the specified part to a project in the second city, but do not print triples in which the two CITY values are the same.

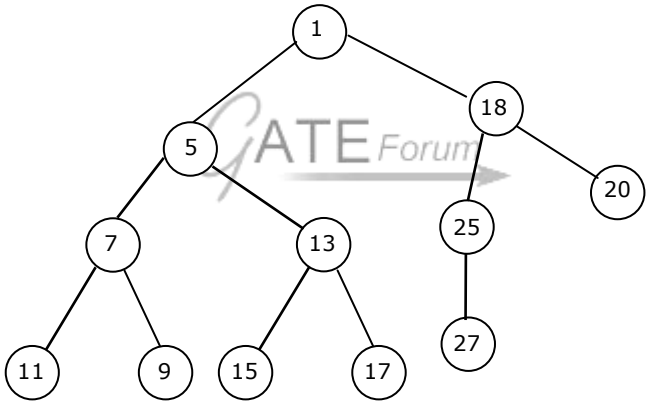
(b) Write algebraic solutions to the following:

(i) Get SCODE values for suppliers who supply to both projects PR1 and PR2.

(ii) Get PRCODE values for projects supplied by at least one supplier not in the same city.

13. Give an optimal algorithm is pseudo-code for sorting a sequence of n numbers which has only k distinct numbers (k is not known a Priori. Give a brief analysis for the time-complexity of your algorithm).

14. Consider the binary tree in Figure:



(a) What structure is represented by the binary tree?

(b) Give the different steps for deleting the node with key 5 so that the structure is preserved.

(c) Outline a procedure in pseudo-code to delete an arbitrary node from such a binary tree with n nodes that preserves the structure. What is the worst-case time-complexity of your procedure?

15. (a) Show that the product of the least common multiple and the greatest common divisor of two positive integers a and b is a*b.

(b) Consider the following first order formula:

$$(Ax)(Ey)R(x,y) \wedge (Ax)(Ay)\big(R(x,y) \rightarrow \sim R(y,x)\big)$$
$$\wedge (Ax)(Ay)(Az)\big(R(x,y) \wedge R(y,z) \rightarrow R(x,z)\big)$$
$$\wedge (Ax) \sim R(x,x)$$

(A-universal quantifier and E-existential quantifier)

Does it have finite models?

Is it satisfiable? Is so, give a countable model for it.

16.

(a) Find the number of binary strings w of length 2n with an equal number os 1's and 0's, and the property that every prefix and w has atleast as many 0's as 1's.

(b) Show that all vertices in an undirected finite graph cannot have distinct degrees, if the graph has at least two vertices.

17. (a) Show that Turing machines, which have a read only input tape and constant size work tape, recognize preasely the class or regular languages.

(b) Let L be the language of all binary strings in which the third symbol from the right is a_1. Give a non-deterministic finite automaton that recognizes L. How many states does the minimized equivalent deterministic finite automaton have? Justify your answer briefly?